

54037072

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006_Jericho2_Control

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014_Jericho2_DRAM_Power

015_Jericho2_GND1

016_Jericho2_GND2

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033_QSFPDD_FAB Port 6 & 8

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037_CLOCK_1

038_CLOCK_2

039_IEEE 1588

040_LED CIRCUIT

041_2X1SFP+ Connector

042_I2C SWITCH_CPLD/QSFPDD_0

043_I2C SWITCH_CPLD/QSFPDD_1

044_CPLD1 10M04DAU324C8G-1

045_CPLD1 10M04DAU324C8G-2

046_CPLD2 10M04DAU324C8G-1

047_CPLD2 10M04DAU324C8G-2

048_CPLD2 10M04DAU324C8G-1

049_CPLD2 10M04DAU324C8G-2

050_I2C DIAGRAM

051_I2C_SYSTEM

052_SCREW

053_SWITCH INT

054_PCIE CONNECTOR_0

055_PCIE CONNECTOR_1

056_CS4227_RESET_CLK_JTAG

057_CS4227_PHY

058_CS4227_POWER

059_PCIE SW SerDes

060_PCIE SW MISC

061_PCIE SW Power & GND

062_SYSTEM LED

063_FAN CONNECTOR

064_POWER CONNECTOR

065_UCD90120A

066_BMC SOCKET0

067_BMC SOCKET1

068_HWM

069_ETH CONTROLLER WGI210AT

070_CONSOLE_OOB_USB

071_PUSH BUTTON &MICRO USB

2072

072_SYSTEM PWR Sequence

073_12V to 5V

074_12V to 3V3/120A_NCP81233

075_12V to 3V3/120A_1-3

076_12V to 3V3/120A_4-6

077_5V to 3V3_CLK

078_3V3 to 2.5V/1.2V

079_3V3 to 1V8/3A

080_12V to 1V2_1/12A

081_12V to 1V2_2/11A

082_12V to 1V2_3/5A

083_12V to 0.9V_VDDM/9A

084_3V3 to 0V88/4A

085_12V to 0.85V/150A_NCP81233

086_12V to 0.85V/150A_1-4

087_12V to 0.85V/150A_5-6

088_12V to 0V8/97A_NCP81233

089_12V to 0V8/97A_1-4

090_12V to ROV/438A_NCP81233

091_12V to ROV/438A_1-4

092_12V to ROV/438A_5-8

093_12V to ROV/438A_9-12

094_3V3 to 3V3_I2C/FAN

095_Coupon Impedence Test

096_12V to 0.9V_PEX/12A

097_3V3 to 0V8_VDDSL/0.75A

098_CPLD POWER

099_3V3 to 0.9V/1A

100_3V3 to 1V8_PHY/3A

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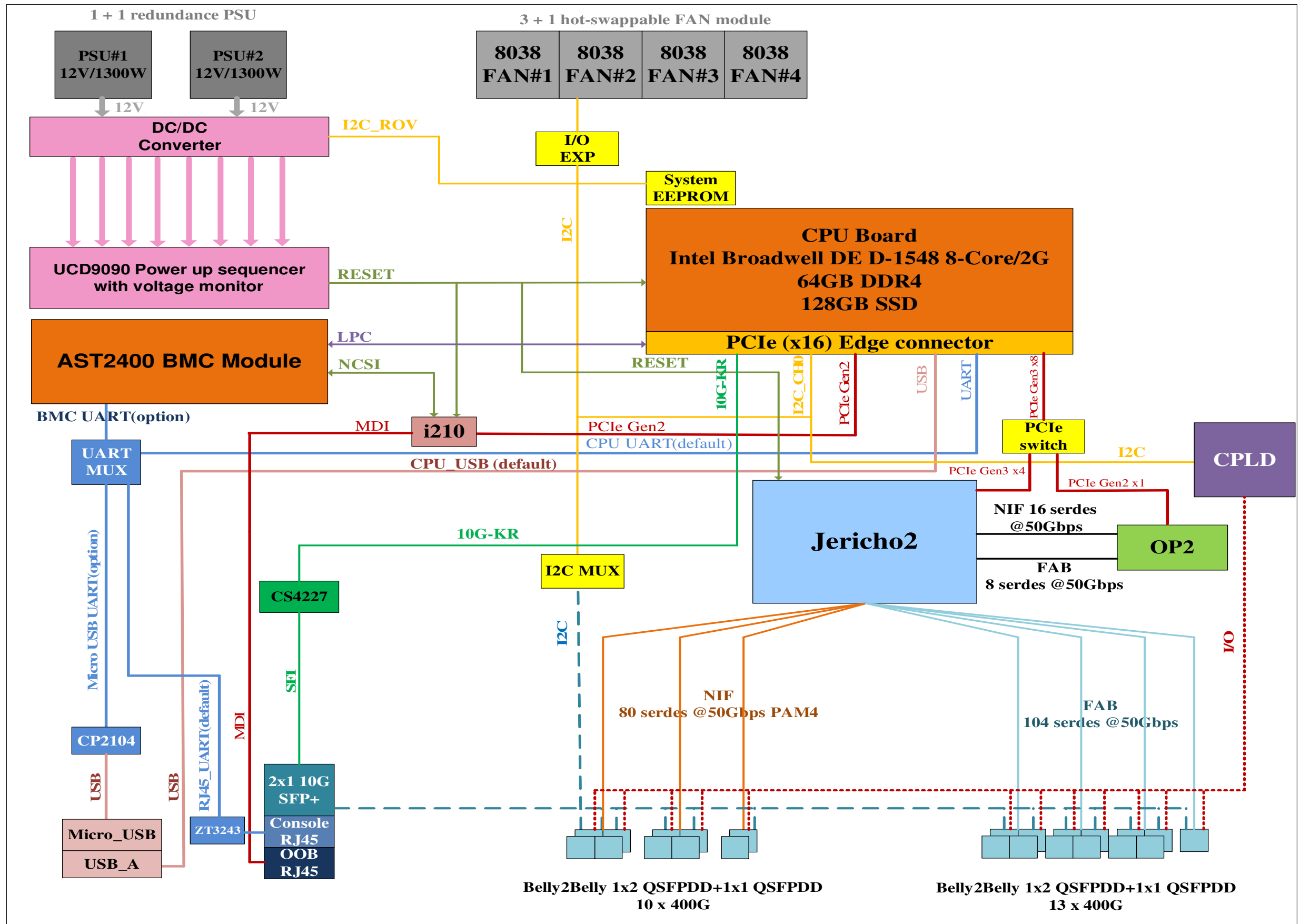
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002_SYSTEM BLOCK DIAGRAM

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(19) FAB_RX_000_N	J45	FAB_RX_000_N	FAB_TX_000_N
(19) FAB_RX_000_P	K45	FAB_RX_000_P	FAB_TX_000_P
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(19) FAB_RX_001_P	F44	FAB_RX_001_P	FAB_TX_001_P
(19) FAB_RX_002_N	J49	FAB_RX_002_N	FAB_TX_002_N
(19) FAB_RX_002_P	K49	FAB_RX_002_P	FAB_TX_002_P
(19) FAB_RX_003_N	G48	FAB_RX_003_N	FAB_TX_003_N
(19) FAB_RX_003_P	F48	FAB_RX_003_P	FAB_TX_003_P
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(19) FAB_RX_007_N	G42	FAB_RX_007_N	FAB_TX_007_N
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(35) FAB_RX_036_P	AE57	FAB_RX_036_P	FAB_TX_036_P
(35) FAB_RX_037_N			
(35) FAB_RX_037_P			

Fabric/ILKN FEC
Connect to OP2

BCM88690

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(35) FAB_RX_038_N	AC57	FAB_RX_038_N	FAB_TX_038_N
(35) FAB_RX_038_P	AC58	FAB_RX_038_P	FAB_TX_038_P
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(35) FAB_RX_039_P	AD60	FAB_RX_039_P	FAB_TX_039_P
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(34) FAB_RX_040_P	AG58	FAB_RX_040_P	FAB_TX_040_P
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FAB_TX_038_N	Y66	FAB_TX_038_N	FAB_TX_038_N
FAB_TX_038_P	Y65	FAB_TX_038_P	FAB_TX_038_P
FAB_TX_039_N	AA63	FAB_TX_039_N	FAB_TX_039_N
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FAB_TX_040_P	AC64	FAB_TX_040_P	FAB_TX_040_P
FAB_TX_041_N	AE63	FAB_TX_041_N	FAB_TX_041_N
FAB_TX_041_P	AD65	FAB_TX_041_P	FAB_TX_041_P
FAB_TX_042_N	AD66	FAB_TX_042_N	FAB_TX_042_N
FAB_TX_042_P	AB66	FAB_TX_042_P	FAB_TX_042_P
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FAB_TX_045_N	AG64	FAB_TX_045_N	FAB_TX_045_N
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FAB_TX_046_N	AH65	FAB_TX_046_N	FAB_TX_046_N
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FAB_TX_051_P	AT65	FAB_TX_051_P	FAB_TX_051_P
FAB_TX_052_N	AT65	FAB_TX_052_N	FAB_TX_052_N
FAB_TX_052_P	AT65	FAB_TX_052_P	FAB_TX_052_P
FAB_TX_053_N	AT66	FAB_TX_053_N	FAB_TX_053_N
FAB_TX_053_P	AR64	FAB_TX_053_P	FAB_TX_053_P
FAB_TX_054_N	AR63	FAB_TX_054_N	FAB_TX_054_N
FAB_TX_054_P	AU63	FAB_TX_054_P	FAB_TX_054_P
FAB_TX_055_N	AU64	FAB_TX_055_N	FAB_TX_055_N
FAB_TX_055_P	CU34	FAB_TX_055_P	FAB_TX_055_P
FAB_TX_056_N	CU34	FAB_TX_056_N	FAB_TX_056_N
FAB_TX_056_P	CE35	FAB_TX_056_P	FAB_TX_056_P
FAB_TX_057_N	CF35	FAB_TX_057_N	FAB_TX_057_N
FAB_TX_057_P	CU36	FAB_TX_057_P	FAB_TX_057_P
FAB_TX_058_N	CU36	FAB_TX_058_N	FAB_TX_058_N
FAB_TX_058_P	CF33	FAB_TX_058_P	FAB_TX_058_P
FAB_TX_059_N	CF33	FAB_TX_059_N	FAB_TX_059_N
FAB_TX_059_P	CD40	FAB_TX_059_P	FAB_TX_059_P
FAB_TX_060_N	CD40	FAB_TX_060_N	FAB_TX_060_N
FAB_TX_060_P	CF39	FAB_TX_060_P	FAB_TX_060_P
FAB_TX_061_N	CF39	FAB_TX_061_N	FAB_TX_061_N
FAB_TX_061_P	CE38	FAB_TX_061_P	FAB_TX_061_P
FAB_TX_062_N	CD38	FAB_TX_062_N	FAB_TX_062_N
FAB_TX_062_P	CF37	FAB_TX_062_P	FAB_TX_062_P
FAB_TX_063_N	CE37	FAB_TX_063_N	FAB_TX_063_N
FAB_TX_063_P	CC42	FAB_TX_063_P	FAB_TX_063_P
FAB_TX_064_N	CD42	FAB_TX_064_N	FAB_TX_064_N
FAB_TX_064_P	CD44	FAB_TX_064_P	FAB_TX_064_P
FAB_TX_065_N	CC44	FAB_TX_065_N	FAB_TX_065_N
FAB_TX_065_P	CE43	FAB_TX_065_P	FAB_TX_065_P
FAB_TX_066_N	CF43	FAB_TX_066_N	FAB_TX_066_N
FAB_TX_066_P	CF41	FAB_TX_066_P	FAB_TX_066_P
FAB_TX_067_N	CE41	FAB_TX_067_N	FAB_TX_067_N
FAB_TX_067_P	CF45	FAB_TX_067_P	FAB_TX_067_P
FAB_TX_068_N	CE45	FAB_TX_068_N	FAB_TX_068_N
FAB_TX_068_P	CB46	FAB_TX_068_P	FAB_TX_068_P
FAB_TX_069_N	CD46	FAB_TX_069_N	FAB_TX_069_N
FAB_TX_069_P	CF47	FAB_TX_069_P	FAB_TX_069_P
FAB_TX_070_N	CE47	FAB_TX_070_N	FAB_TX_070_N
FAB_TX_070_P	CC48	FAB_TX_070_P	FAB_TX_070_P
FAB_TX_071_N	CD48	FAB_TX_071_N	FAB_TX_071_N
FAB_TX_071_P	CC50	FAB_TX_071_P	FAB_TX_071_P
FAB_TX_072_N	CC50	FAB_TX_072_N	FAB_TX_072_N
FAB_TX_072_P	CD52	FAB_TX_072_P	FAB_TX_072_P
FAB_TX_073_N	CE51	FAB_TX_073_N	FAB_TX_073_N
FAB_TX_073_P	CF51	FAB_TX_073_P	FAB_TX_073_P
FAB_TX_074_N	CF49	FAB_TX_074_N	FAB_TX_074_N
FAB_TX_074_P	CE49	FAB_TX_074_P	FAB_TX_074_P
FAB_TX_075_N			
FAB_TX_075_P			

FAB_TX_038_N	FAB_TX_038_N	(35)	FAB_TX_038_N
FAB_TX_038_P	FAB_TX_038_P	(35)	FAB_TX_038_P
FAB_TX_039_N	FAB_TX_039_N	(35)	FAB_TX_039_N
FAB_TX_039_P	FAB_TX_039_P	(35)	FAB_TX_039_P
FAB_TX_040_N	FAB_TX_040_N	(34)	FAB_TX_040_N
FAB_TX_040_P	FAB_TX_040_P	(34)	FAB_TX_040_P
FAB_TX_041_N	FAB_TX_041_N	(34)	FAB_TX_041_N
FAB_TX_041_P	FAB_TX_041_P	(34)	FAB_TX_041_P
FAB_TX_042_N	FAB_TX_042_N	(34)	FAB_TX_042_N
FAB_TX_042_P	FAB_TX_042_P	(34)	FAB_TX_042_P
FAB_TX_043_N	FAB_TX_043_N	(34)	FAB_TX_043_N
FAB_TX_043_P	FAB_TX_043_P	(34)	FAB_TX_043_P
FAB_TX_044_N	FAB_TX_044_N	(34)	FAB_TX_044_N
FAB_TX_044_P	FAB_TX_044_P	(34)	FAB_TX_044_P
FAB_TX_045_N	FAB_TX_045_N	(34)	FAB_TX_045_N
FAB_TX_045_P	FAB_TX_045_P	(34)	FAB_TX_045_P
FAB_TX_046_N	FAB_TX_046_N	(34)	FAB_TX_046_N
FAB_TX_046_P	FAB_TX_046_P	(34)	FAB_TX_046_P
FAB_TX_047_N	FAB_TX_047_N	(34)	FAB_TX_

U26D

(24) NIF_RX_00_N	N9	NIF_RX_00_N
(24) NIF_RX_00_P	N10	NIF_RX_00_P
(24) NIF_RX_01_N	M7	NIF_RX_01_N
(24) NIF_RX_01_P	M6	NIF_RX_01_P
(24) NIF_RX_02_N	L9	NIF_RX_02_N
(24) NIF_RX_02_P	L10	NIF_RX_02_P
(24) NIF_RX_03_N	K13	NIF_RX_03_N
(24) NIF_RX_03_P	K12	NIF_RX_03_P
(24) NIF_RX_04_N	P7	NIF_RX_04_N
(24) NIF_RX_04_P	P6	NIF_RX_04_P
(24) NIF_RX_05_N	R9	NIF_RX_05_N
(24) NIF_RX_05_P	R10	NIF_RX_05_P
(24) NIF_RX_06_N	M13	NIF_RX_06_N
(24) NIF_RX_06_P	M12	NIF_RX_06_P
(24) NIF_RX_07_N	P12	NIF_RX_07_N
(24) NIF_RX_07_P	P13	NIF_RX_07_P
(25) NIF_RX_08_N	U9	NIF_RX_08_N
(25) NIF_RX_08_P	U10	NIF_RX_08_P
(25) NIF_RX_09_N	T13	NIF_RX_09_N
(25) NIF_RX_09_P	T12	NIF_RX_09_P
(25) NIF_RX_10_N	V13	NIF_RX_10_N
(25) NIF_RX_10_P	V12	NIF_RX_10_P
(25) NIF_RX_11_N	T7	NIF_RX_11_N
(25) NIF_RX_11_P	T6	NIF_RX_11_P
(25) NIF_RX_12_N	Y7	NIF_RX_12_N
(25) NIF_RX_12_P	Y6	NIF_RX_12_P
(25) NIF_RX_13_N	AB6	NIF_RX_13_N
(25) NIF_RX_13_P	AB7	NIF_RX_13_P
(25) NIF_RX_14_N	V7	NIF_RX_14_N
(25) NIF_RX_14_P	V6	NIF_RX_14_P
(25) NIF_RX_15_N	W9	NIF_RX_15_N
(25) NIF_RX_15_P	W10	NIF_RX_15_P
(24) NIF_RX_16_N	AD12	NIF_RX_16_N
(24) NIF_RX_16_P	AD13	NIF_RX_16_P
(24) NIF_RX_17_N	AB13	NIF_RX_17_N
(24) NIF_RX_17_P	AB12	NIF_RX_17_P
(24) NIF_RX_18_N	AA9	NIF_RX_18_N
(24) NIF_RX_18_P	AA10	NIF_RX_18_P
(24) NIF_RX_19_N	Y13	NIF_RX_19_N
(24) NIF_RX_19_P	Y12	NIF_RX_19_P
(24) NIF_RX_20_N	AC10	NIF_RX_20_N
(24) NIF_RX_20_P	AC9	NIF_RX_20_P
(24) NIF_RX_21_N	AE9	NIF_RX_21_N
(24) NIF_RX_21_P	AE10	NIF_RX_21_P
(24) NIF_RX_22_N	AD7	NIF_RX_22_N
(24) NIF_RX_22_P	AD6	NIF_RX_22_P
(24) NIF_RX_23_N	AF6	NIF_RX_23_N
(24) NIF_RX_23_P	AF7	NIF_RX_23_P
(25) NIF_RX_24_N	AJ9	NIF_RX_24_N
(25) NIF_RX_24_P	AJ10	NIF_RX_24_P
(25) NIF_RX_25_N	AG10	NIF_RX_25_N
(25) NIF_RX_25_P	AG9	NIF_RX_25_P
(25) NIF_RX_26_N	AH12	NIF_RX_26_N
(25) NIF_RX_26_P	AH13	NIF_RX_26_P
(25) NIF_RX_27_N	AF13	NIF_RX_27_N
(25) NIF_RX_27_P	AH7	NIF_RX_27_P
(25) NIF_RX_28_N	AH6	NIF_RX_28_N
(25) NIF_RX_28_P	AK6	NIF_RX_28_P
(25) NIF_RX_29_N	AK7	NIF_RX_29_N
(25) NIF_RX_29_P	AL10	NIF_RX_29_P
(25) NIF_RX_30_N	AL9	NIF_RX_30_N
(25) NIF_RX_31_N	AM6	NIF_RX_31_N
(25) NIF_RX_31_P	AM7	NIF_RX_31_P
(26) NIF_RX_32_N	AN9	NIF_RX_32_N
(26) NIF_RX_32_P	AN10	NIF_RX_32_P
(26) NIF_RX_33_N	AM13	NIF_RX_33_N
(26) NIF_RX_33_P	AM12	NIF_RX_33_P
(26) NIF_RX_34_N	AP12	NIF_RX_34_N
(26) NIF_RX_34_P	AK13	NIF_RX_34_P
(26) NIF_RX_35_N	AK12	NIF_RX_35_N
(26) NIF_RX_35_P	AP7	NIF_RX_35_P
(26) NIF_RX_36_N	AP6	NIF_RX_36_N
(26) NIF_RX_36_P	AR9	NIF_RX_36_P
(26) NIF_RX_37_N	AR10	NIF_RX_37_N
(26) NIF_RX_37_P	AT7	NIF_RX_37_P
(26) NIF_RX_38_N	AT6	NIF_RX_38_N
(26) NIF_RX_38_P	AU9	NIF_RX_38_P
(26) NIF_RX_39_N	AU10	NIF_RX_39_N
(27) NIF_RX_40_N	AW9	NIF_RX_40_N
(27) NIF_RX_40_P	AW10	NIF_RX_40_P
(27) NIF_RX_41_N	AV7	NIF_RX_41_N
(27) NIF_RX_41_P	AV12	NIF_RX_41_P
(27) NIF_RX_42_N	AV13	NIF_RX_42_N
(27) NIF_RX_42_P	AT13	NIF_RX_42_P
(27) NIF_RX_43_N	AT12	NIF_RX_43_N
(27) NIF_RX_43_P	AY7	NIF_RX_43_P
(27) NIF_RX_44_N	AY6	NIF_RX_44_N
(27) NIF_RX_44_P	BA9	NIF_RX_44_P
(27) NIF_RX_45_N	BA10	NIF_RX_45_N
(27) NIF_RX_45_P	BB7	NIF_RX_45_P
(27) NIF_RX_46_N	BB6	NIF_RX_46_N
(27) NIF_RX_46_P	AY13	NIF_RX_46_P
(27) NIF_RX_47_N	AY12	NIF_RX_47_N
(27) NIF_RX_47_P		

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NIF_TX_00_N	B14
NIF_TX_00_P	A14
NIF_TX_01_N	C15
NIF_TX_01_P	D15
NIF_TX_02_N	D17
NIF_TX_02_P	C17
NIF_TX_03_N	B16
NIF_TX_03_P	C21
NIF_TX_04_N	D21
NIF_TX_04_P	B20
NIF_TX_05_N	A20
NIF_TX_05_P	C19
NIF_TX_06_N	B18
NIF_TX_06_P	A18
NIF_TX_07_N	D1
NIF_TX_07_P	D2
NIF_TX_08_N	F2
NIF_TX_08_P	F1
NIF_TX_09_N	G4
NIF_TX_09_P	E4
NIF_TX_10_N	E3
NIF_TX_10_P	H2
NIF_TX_11_N	H1
NIF_TX_11_P	J3
NIF_TX_12_N	J4
NIF_TX_12_P	K2
NIF_TX_13_N	K1
NIF_TX_13_P	L3
NIF_TX_14_N	L4
NIF_TX_14_P	N4
NIF_TX_15_N	N3
NIF_TX_15_P	P2
NIF_TX_16_N	R4
NIF_TX_16_P	R3
NIF_TX_17_N	M1
NIF_TX_17_P	M2
NIF_TX_18_N	T1
NIF_TX_18_P	U4
NIF_TX_19_N	U3
NIF_TX_19_P	V1
NIF_TX_20_N	V2
NIF_TX_20_P	W4
NIF_TX_21_N	W3
NIF_TX_21_P	AA4
NIF_TX_22_N	AA3
NIF_TX_22_P	AB1
NIF_TX_23_N	AB2
NIF_TX_23_P	AC4
NIF_TX_24_N	AC3
NIF_TX_24_P	Y1
NIF_TX_25_N	Y2
NIF_TX_25_P	AD1
NIF_TX_26_N	AD2
NIF_TX_26_P	AE4
NIF_TX_27_N	AE3
NIF_TX_27_P	AF1
NIF_TX_28_N	AF2
NIF_TX_28_P	AG4
NIF_TX_29_N	AG3
NIF_TX_29_P	AJ4
NIF_TX_30_N	AJ3
NIF_TX_30_P	AL3
NIF_TX_31_N	AL4
NIF_TX_31_P	AK2
NIF_TX_32_N	AK1
NIF_TX_32_P	AH1
NIF_TX_33_N	AH2
NIF_TX_33_P	AM1
NIF_TX_34_N	AM2
NIF_TX_34_P	AN4
NIF_TX_35_N	AN3
NIF_TX_35_P	AP2
NIF_TX_36_N	AR4
NIF_TX_36_P	AR3
NIF_TX_37_N	AU4
NIF_TX_37_P	AU3
NIF_TX_38_N	AW3
NIF_TX_38_P	AW4
NIF_TX_39_N	AV2
NIF_TX_39_P	AV1
NIF_TX_40_N	AT1
NIF_TX_40_P	AT2
NIF_TX_41_N	AY1
NIF_TX_41_P	AY2
NIF_TX_42_N	BA4
NIF_TX_42_P	BA3
NIF_TX_43_N	BB1
NIF_TX_43_P	BB2
NIF_TX_44_N	BC4
NIF_TX_44_P	BC3

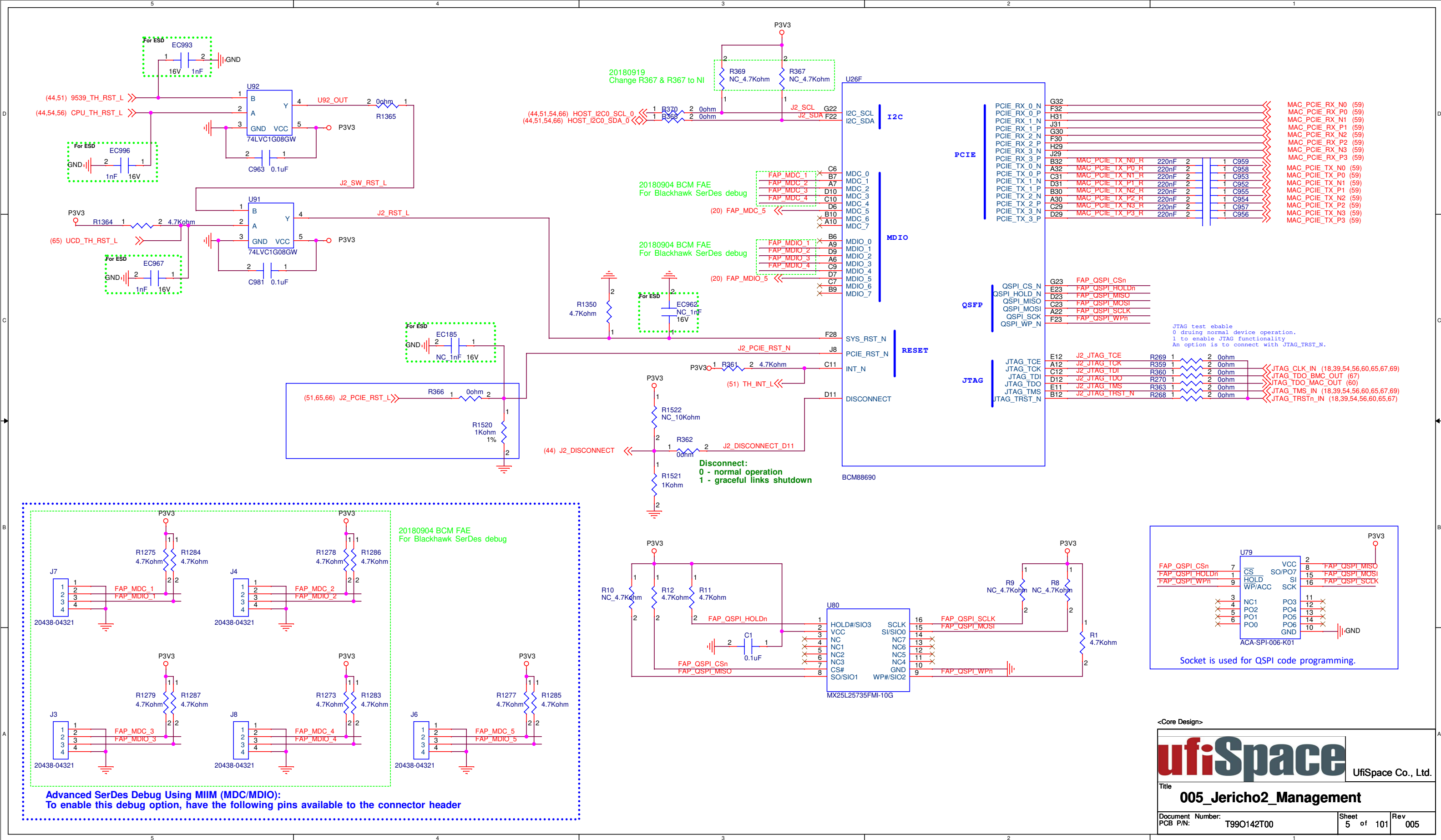
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NIF_TX_03_N (24)	
NIF_TX_03_P (24)	
NIF_TX_04_N (24)	
NIF_TX_04_P (24)	
NIF_TX_05_N (24)	
NIF_TX_05_P (24)	
NIF_TX_06_N (24)	
NIF_TX_06_P (24)	
NIF_TX_07_N (24)	
NIF_TX_07_P (24)	
NIF_TX_08_N (25)	
NIF_TX_08_P (25)	
NIF_TX_09_N (25)	
NIF_TX_09_P (25)	
NIF_TX_10_N (25)	
NIF_TX_10_P (25)	
NIF_TX_11_N (25)	
NIF_TX_11_P (25)	
NIF_TX_12_N (25)	
NIF_TX_12_P (25)	
NIF_TX_13_N (25)	
NIF_TX_13_P (25)	
NIF_TX_14_N (25)	
NIF_TX_14_P (25)	
NIF_TX_15_N (25)	
NIF_TX_15_P (25)	
NIF_TX_16_N (24)	
NIF_TX_16_P (24)	
NIF_TX_17_N (24)	
NIF_TX_17_P (24)	
NIF_TX_18_N (24)	
NIF_TX_18_P (24)	
NIF_TX_19_N (24)	
NIF_TX_19_P (24)	
NIF_TX_20_N (24)	
NIF_TX_20_P (24)	
NIF_TX_21_N (24)	
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NIF_TX_22_N (24)	
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NIF_TX_23_P (24)	
NIF_TX_24_N (25)	
NIF_TX_24_P (25)	
NIF_TX_25_N (25)	
NIF_TX_25_P (25)	
NIF_TX_26_N (25)	
NIF_TX_26_P (25)	
NIF_TX_27_N (25)	
NIF_TX_27_P (25)	
NIF_TX_28_N (25)	
NIF_TX_28_P (25)	
NIF_TX_29_N (25)	
NIF_TX_29_P (25)	
NIF_TX_30_N (25)	
NIF_TX_30_P (25)	
NIF_TX_31_N (25)	
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NIF_TX_35_P (26)	
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NIF_TX_36_P (26)	
NIF_TX_37_N (26)	
NIF_TX_37_P (26)	
NIF_TX_38_N (26)	
NIF_TX_38_P (26)	
NIF_TX_39_N (26)	
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NIF_TX_40_N (27)	
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NIF_TX_41_N (27)	
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NIF_TX_42_P (27)	
NIF_TX_43_N (27)	
NIF_TX_43_P (27)	
NIF_TX_44_N (27)	
NIF_TX_44_P (27)	
NIF_TX_45_N (27)	
NIF_TX_45_P (27)	
NIF_TX_46_N (27)	
NIF_TX_46_P (27)	
NIF_TX_47_N (27)	
NIF_TX_47_P (27)	

NIF/ILKN FEC
Connect to OP2

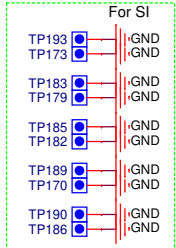
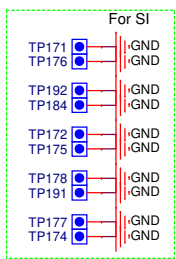
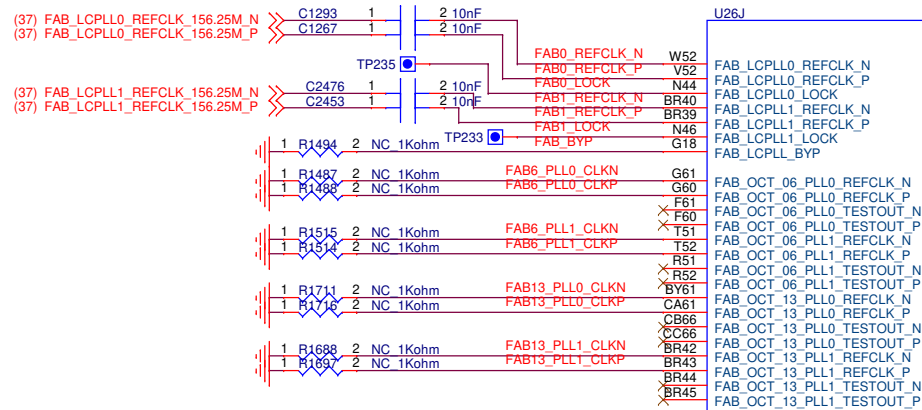
(19) NIF_RX_48_N	CA29
(19) NIF_RX_48_P	BY29
(19) NIF_RX_49_N	BU28
(19) NIF_RX_49_P	BV28
(19) NIF_RX_50_N	CA27
(19) NIF_RX_50_P	BY27
(19) NIF_RX_51_N	BU26
(19) NIF_RX_51_P	BV26
(19) NIF_RX_52_N	BU30
(19) NIF_RX_52_P	BV30
(19) NIF_RX_53_N	CA31
(19) NIF_RX_53_P	BY31
(19) NIF_RX_54_N	BU32
(19) NIF_RX_54_P	CA33
(19) NIF_RX_55_N	BY33
(19) NIF_RX_55_P	BV22
(19) NIF_RX_56_N	BU22
(19) NIF_RX_56_P	BY23
(19) NIF_RX_57_N	CA23
(19) NIF_RX_57_P	CA25
(19) NIF_RX_58_N	CA25
(19) NIF_RX_58_P	BV24
(19) NIF_RX_59_N	BU24
(19) NIF_RX_59_P	BY21
(19) NIF_RX_60_N	CA21
(19) NIF_RX_60_P	BV20
(19) NIF_RX_61_N	BY19
(19) NIF_RX_61_P	CA19
(19) NIF_RX_62_N	BV18
(19) NIF_RX_62_P	BU18
(19) NIF_RX_63_N	CA13
(19) NIF_RX_63_P	BY13
(29) NIF_RX_64_N	BY15
(29) NIF_RX_64_P	CA15
(29) NIF_RX_65_N	CA15
(29) NIF_RX_65_P	BV16
(29) NIF_RX_66_N	BU16
(29) NIF_RX_66_P	BY17
(29) NIF_RX_67_N	CA17
(29) NIF_RX_67_P	BU14
(29) NIF_RX_68_N	BV14
(29) NIF_RX_68_P	BY12
(29) NIF_RX_69_N	BY11
(29) NIF_RX_69_P	CA11
(29) NIF_RX_70_N	CA9
(29) NIF_RX_70_P	BY9
(29) NIF_RX_71_N	BV9
(29) NIF_RX_71_P	BU9
(28) NIF_RX_72_N	B17
(28) NIF_RX_72_P	BU10
(28) NIF_RX_73_N	BU9
(28) NIF_RX_73_P	BV6
(28) NIF_RX_74_N	BV7
(28) NIF_RX_74_P	BY7
(28) NIF_RX_75_N	CA7
(28) NIF_RX_75_P	BP13
(28) NIF_RX_76_N	BP12
(28) NIF_RX_76_P	BM12
(28) NIF_RX_77_N	BM13
(28) NIF_RX_77_P	BR10
(28) NIF_RX_78_N	BR9
(28) NIF_RX_78_P	BN10
(28) NIF_RX_79_N	BL9
(28) NIF_RX_79_P	BL10
(27) NIF_RX_80_N	BK13
(27) NIF_RX_80_P	BK12
(27) NIF_RX_81_N	BM6
(27) NIF_RX_81_P	BP7
(27) NIF_RX_82_N	BP6
(27) NIF_RX_82_P	BK7
(27) NIF_RX_83_N	BK6
(27) NIF_RX_83_P	BF12
(27) NIF_RX_84_N	BF13
(27) NIF_RX_84_P	BH13
(27) NIF_RX_85_N	BH12
(27) NIF_RX_85_P	BJ9
(27) NIF_RX_86_N	BJ10
(27) NIF_RX_86_P	BD6
(27) NIF_RX_87_N	BD7
(26) NIF_RX_88_N	BF7
(26) NIF_RX_88_P	BF6
(26) NIF_RX_89_N	BG9
(26) NIF_RX_89_P	BG10
(26) NIF_RX_90_N	BH7
(26) NIF_RX_90_P	BH6
(26) NIF_RX_91_N	BB13
(26) NIF_RX_91_P	BB12
(26) NIF_RX_92_N	BE10
(26) NIF_RX_92_P	BE9
(26) NIF_RX_93_N	BD12
(26) NIF_RX_93_P	BD13
(26) NIF_RX_94_N	
(26) NIF_RX_94_P	
(26) NIF_RX_95_N	
(26) NIF_RX_95_P	

U26E

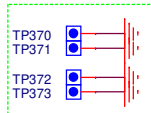
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NIF_RX_48_P	CD28
NIF_RX_49_N	CF27
NIF_RX_49_P	CE27
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NIF_RX_50_P	CD26
NIF_RX_51_N	CF25
NIF_RX_51_P	CE25
NIF_RX_52_N	CF29
NIF_RX_52_P	CE29
NIF_RX_53_N	CC30
NIF_RX_53_P	CD30
NIF_RX_54_N	CF31
NIF_RX_54_P	CE31
NIF_RX_55_N	CC32
NIF_RX_55_P	CD32
NIF_RX_56_N	CF23
NIF_RX_56_P	CE23
NIF_RX_57_N	CF21
NIF_RX_57_P	CE21
NIF_RX_58_N	CD22
NIF_RX_58_P	CE22
NIF_RX_59_N	CC24
NIF_RX_59_P	CD24
NIF_RX_60_N	CC20
NIF_RX_60_P	CD20
NIF_RX_61_N	CE19
NIF_RX_61_P	CF19
NIF_RX_62_N	CE17
NIF_RX_62_P	CF17
NIF_RX_63_N	CE18
NIF_RX_63_P	CF18
NIF_RX_64_N	CD18
NIF_RX_64_P	CE16
NIF_RX_65_N	CD16
NIF_RX_65_P	CE14
NIF_RX_66_N	CC14
NIF_RX_66_P	CE13
NIF_RX_67_N	CF13
NIF_RX_67_P	CE15
NIF_RX_68_N	CF11
NIF_RX_68_P	CE11
NIF_RX_69_N	CC12
NIF_RX_69_P	CD12
NIF_RX_70_N	CF9
NIF_RX_70_P	CE9
NIF_RX_71_N	CC10
NIF_RX_71_P	CD10
NIF_RX_72_N	BY2
NIF_RX_72_P	CD8
NIF_RX_73_N	CD6
NIF_RX_73_P	CC6
NIF_RX_74_N	CE5
NIF_RX_74_P	CF5
NIF_RX_75_N	CF7
NIF_RX_75_P	CE7
NIF_RX_76_N	CC3
NIF_RX_76_P	CC4
NIF_RX_77_N	CB2
NIF_RX_77_P	CB1
NIF_RX_78_N	CA3
NIF_RX_78_P	CA4
NIF_RX_79_N	BY2
NIF_RX_79_P	BY1
NIF_RX_80_N	BV2
NIF_RX_80_P	BT1
NIF_RX_81_N	BT2
NIF_RX_81_P	BU4
NIF_RX_82_N	BU3
NIF_RX_82_P	BW3
NIF_RX_83_N	BW4
NIF_RX_83_P	BR3
NIF_RX_84_N	BR4
NIF_RX_84_P	BP2
NIF_RX_85_N	BP1
NIF_RX_85_P	BN4
NIF_RX_86_N	BM2
NIF_RX_86_P	BM1
NIF_RX_87_N	BK2
NIF_RX_87_P	BK1
NIF_RX_88_N	BH1
NIF_RX_88_P	BH2
NIF_RX_89_N	BL3
NIF_RX_89_P	BL4
NIF_RX_90_N	EG3
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NIF_RX_92_N	BE4
NIF_RX_92_P	



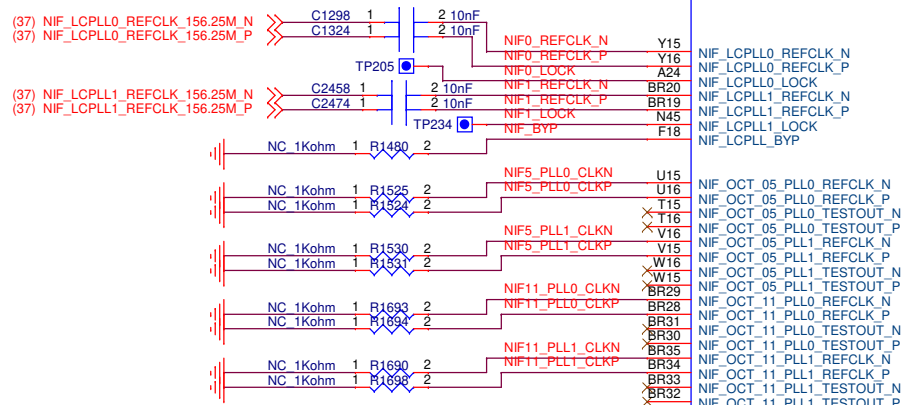
20180904
Add GND test point to RMS Jitter measure



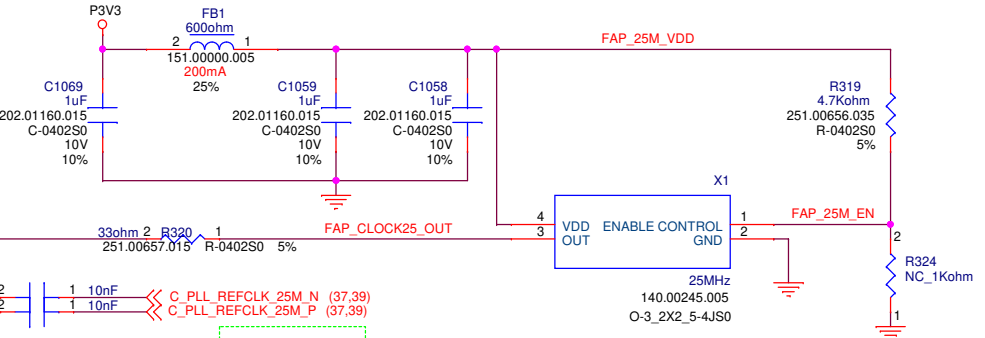
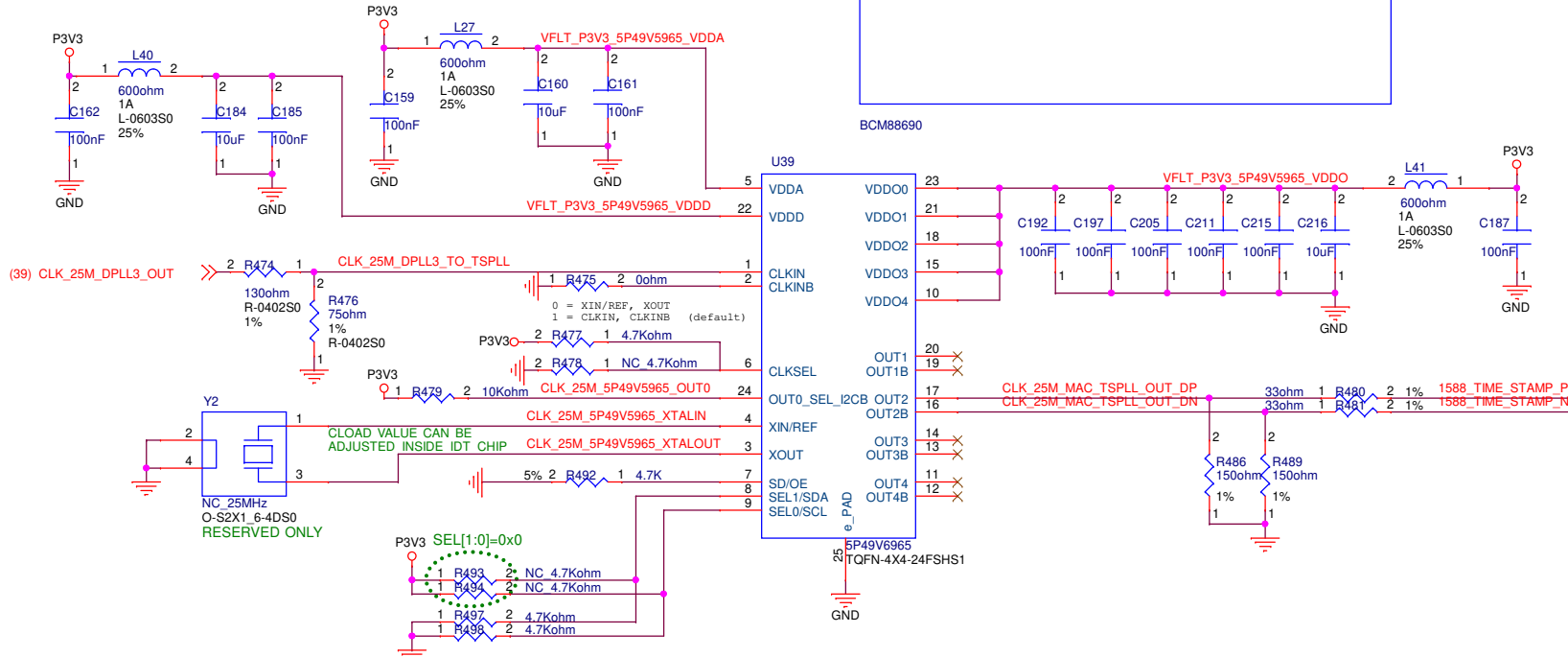
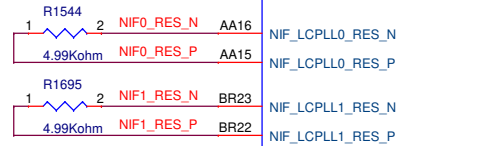
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Add GND test point to RMS Jitter measure



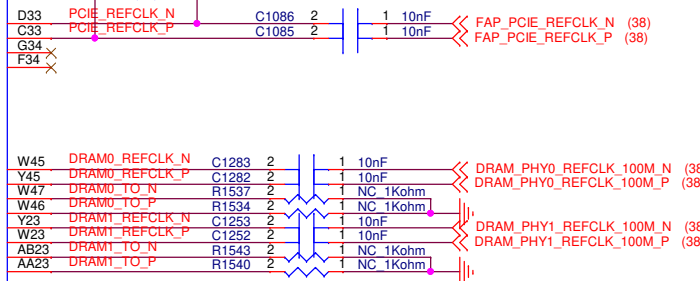
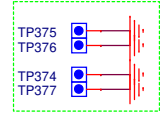
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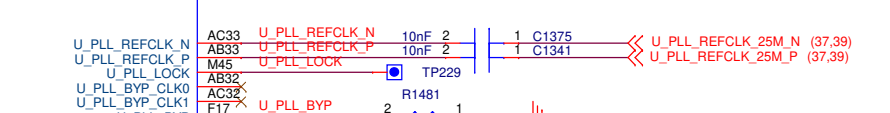
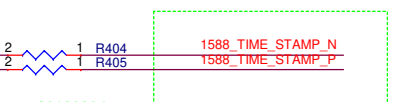
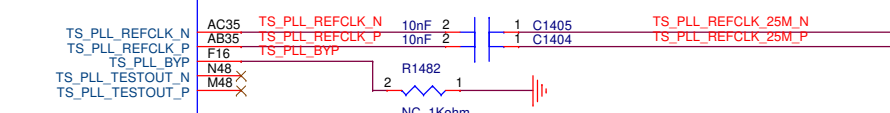
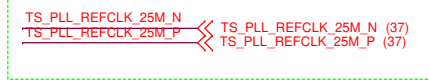
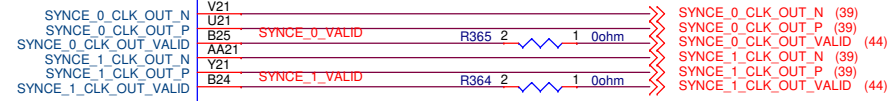
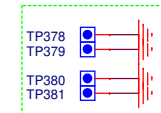
Place under the BGA



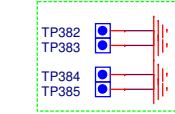
20180904
Add GND test point to RMS Jitter measure



20180904
Add GND test point to RMS Jitter measure



20180904
Add GND test point to RMS Jitter measure



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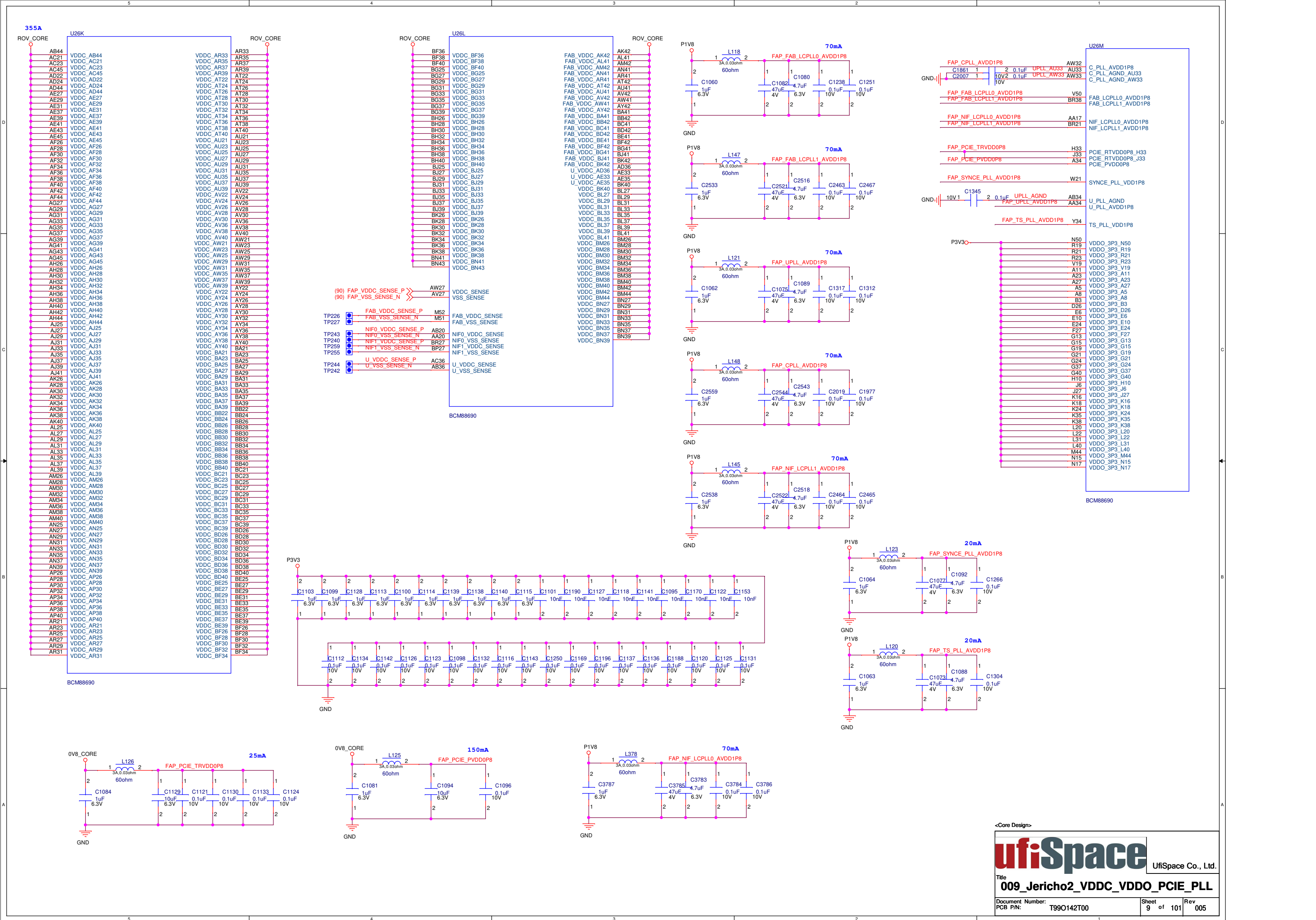
UfiSpace Co., Ltd.

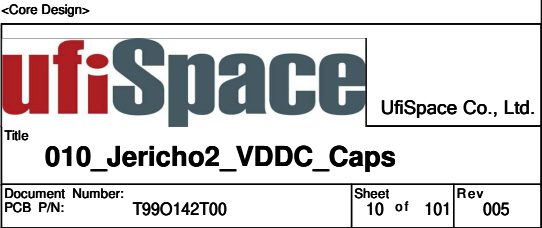
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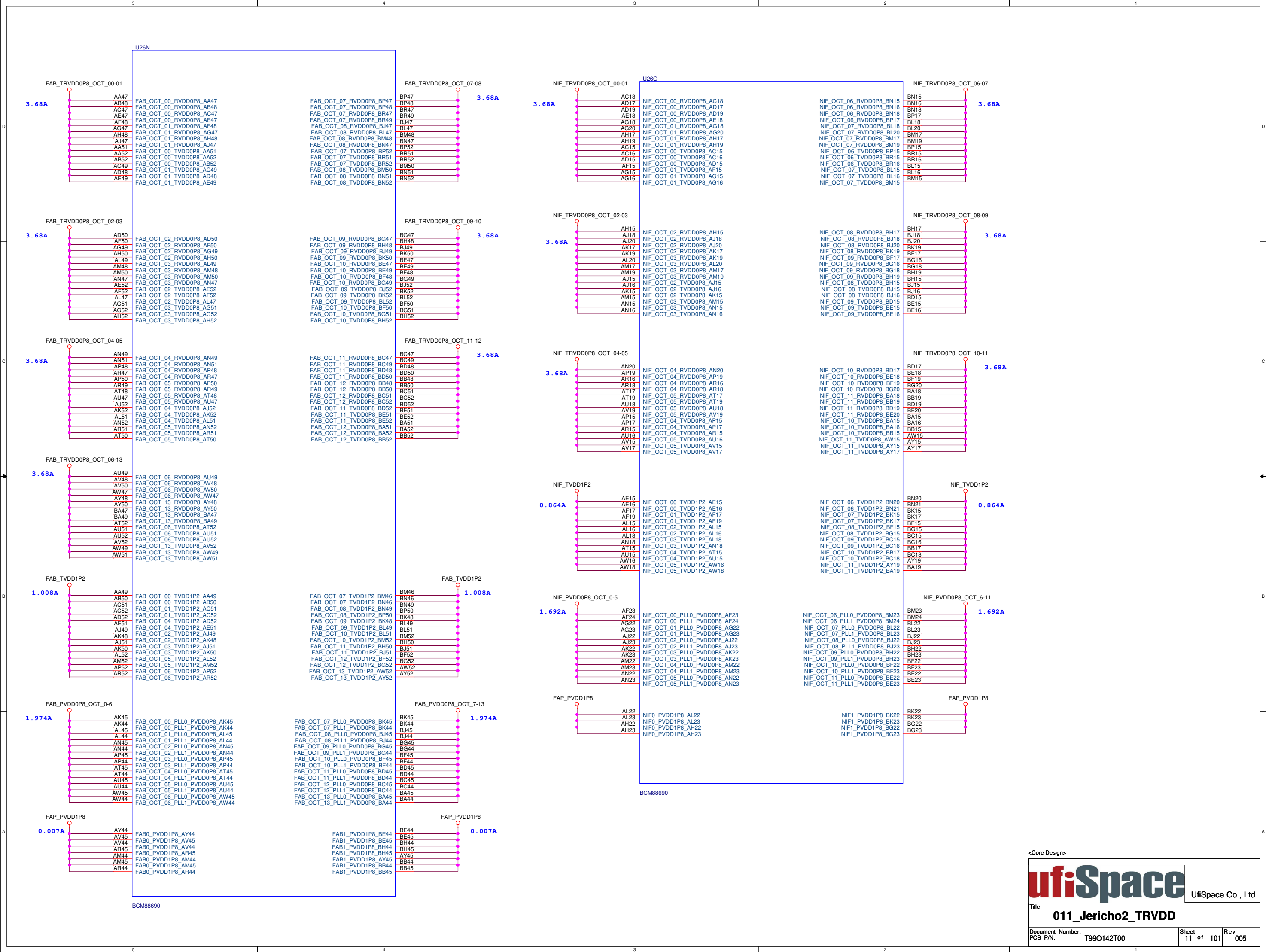
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PCB P/N: T990142T00

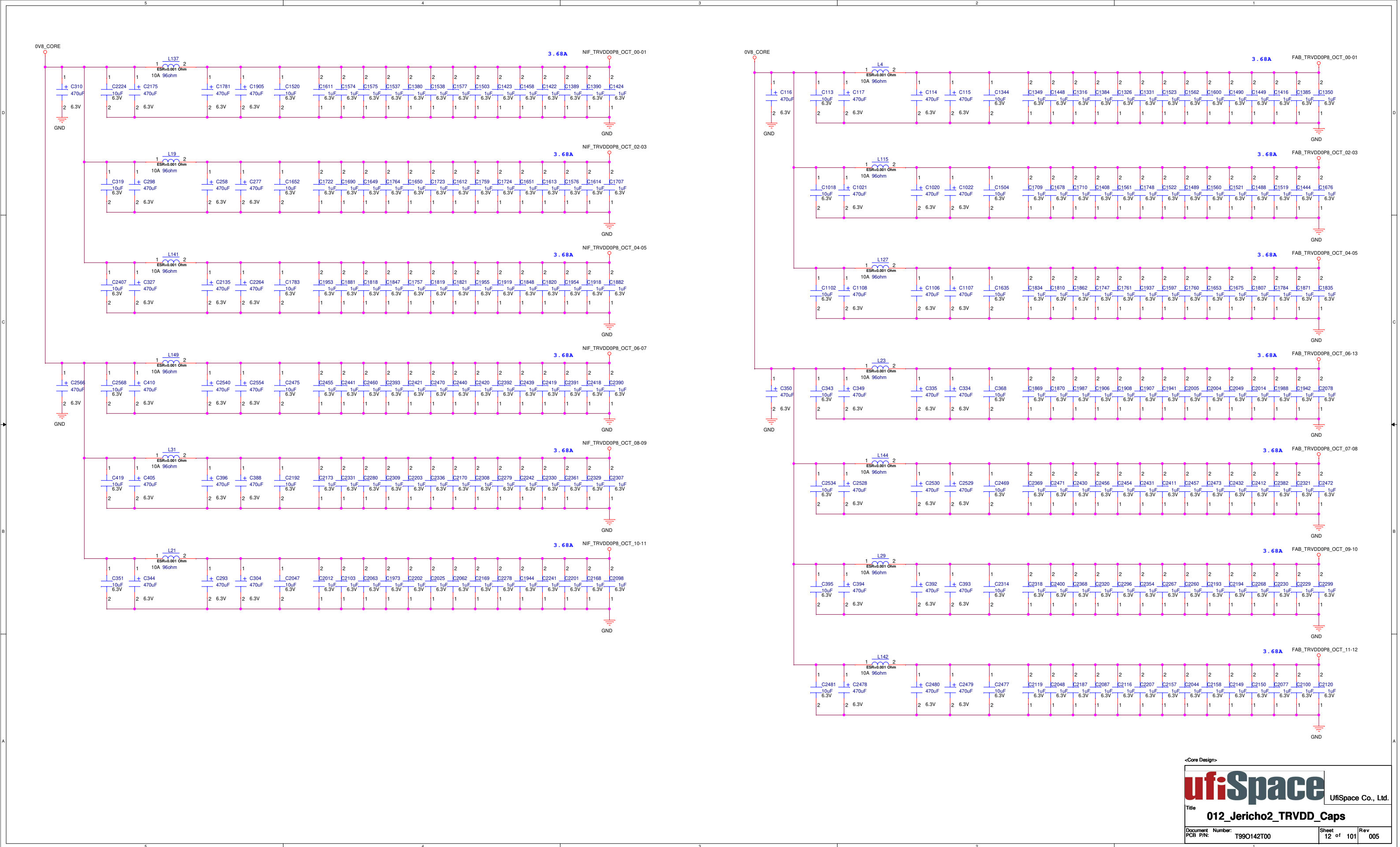
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8 of 101

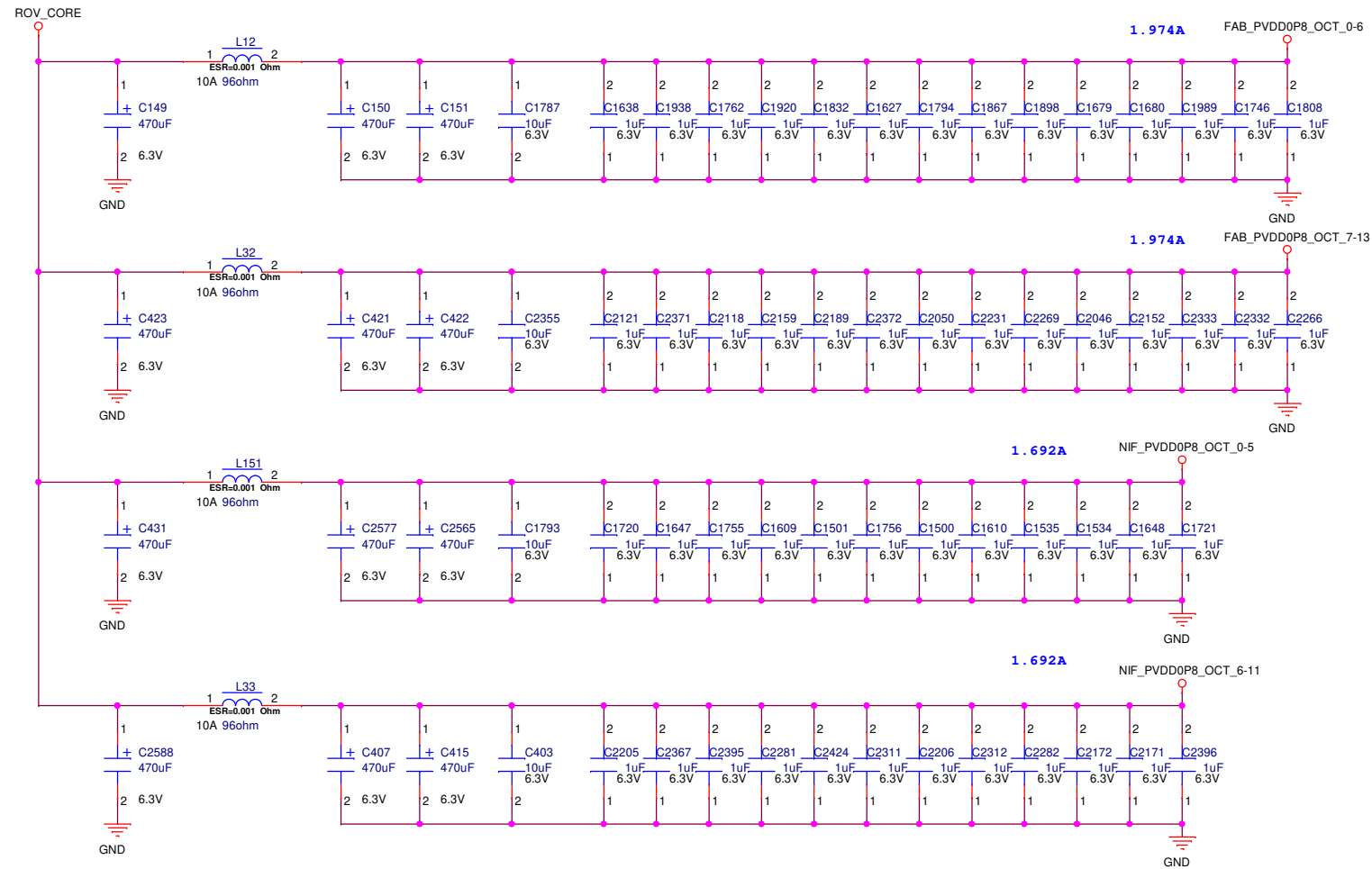
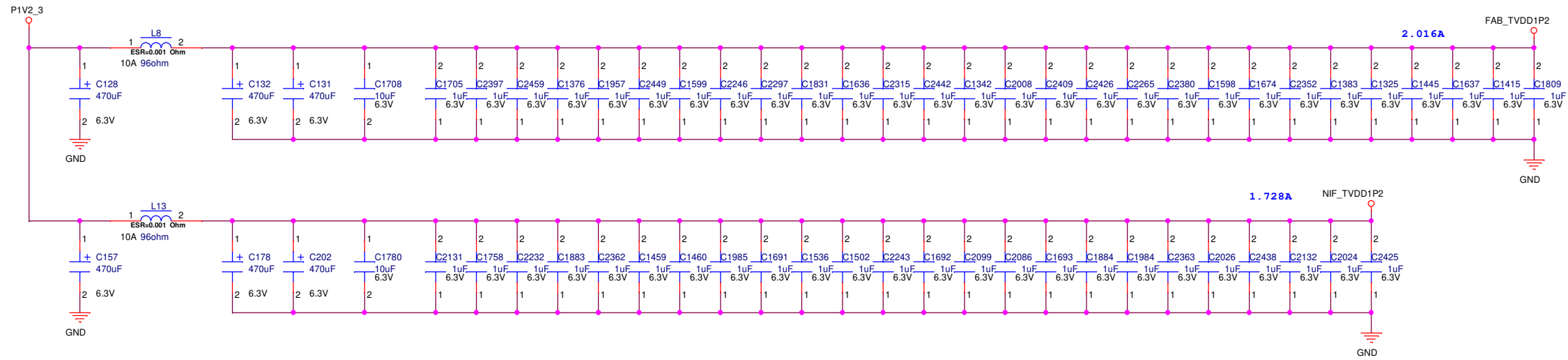
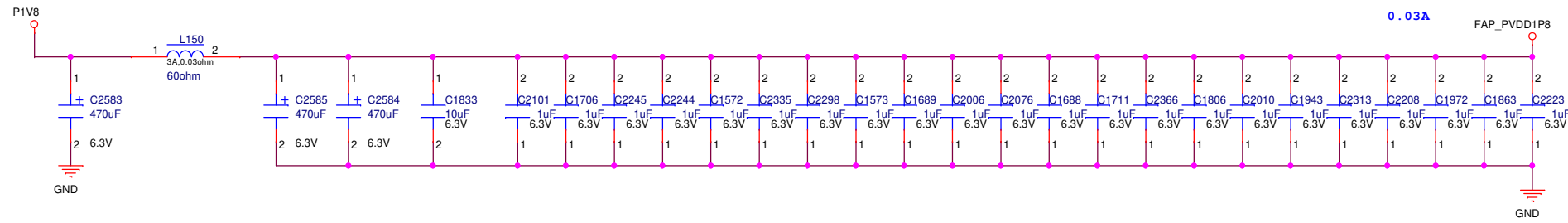
Rev
005



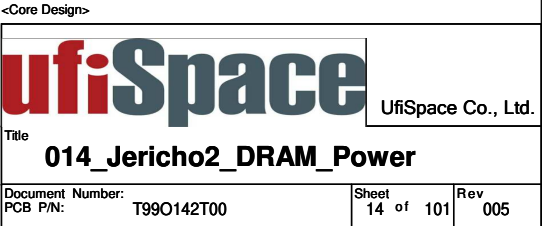


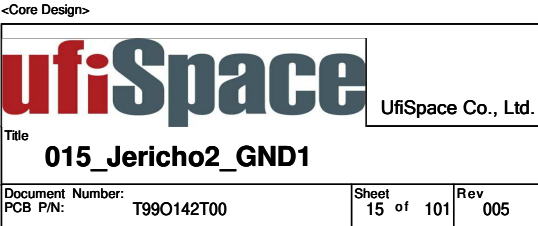


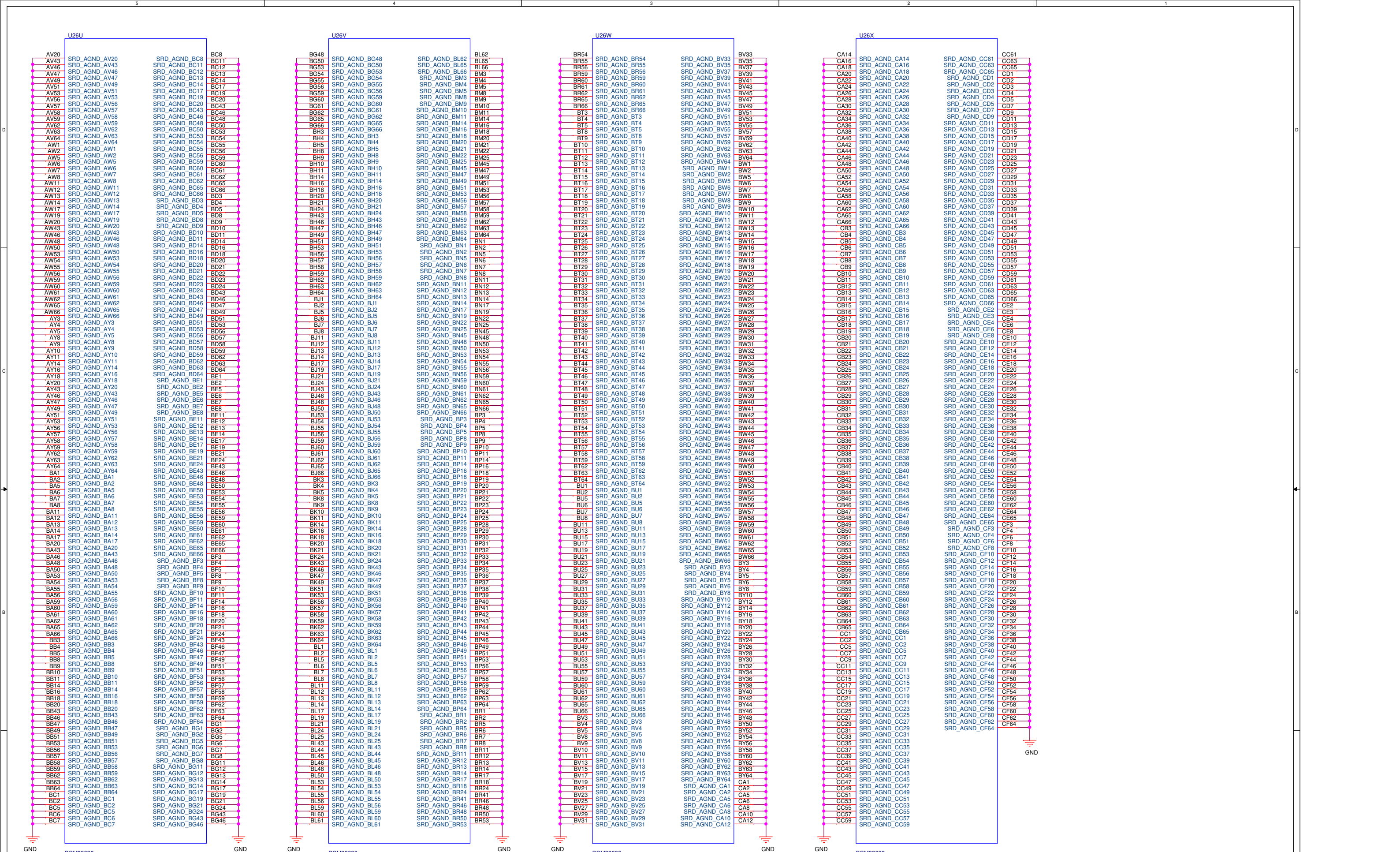


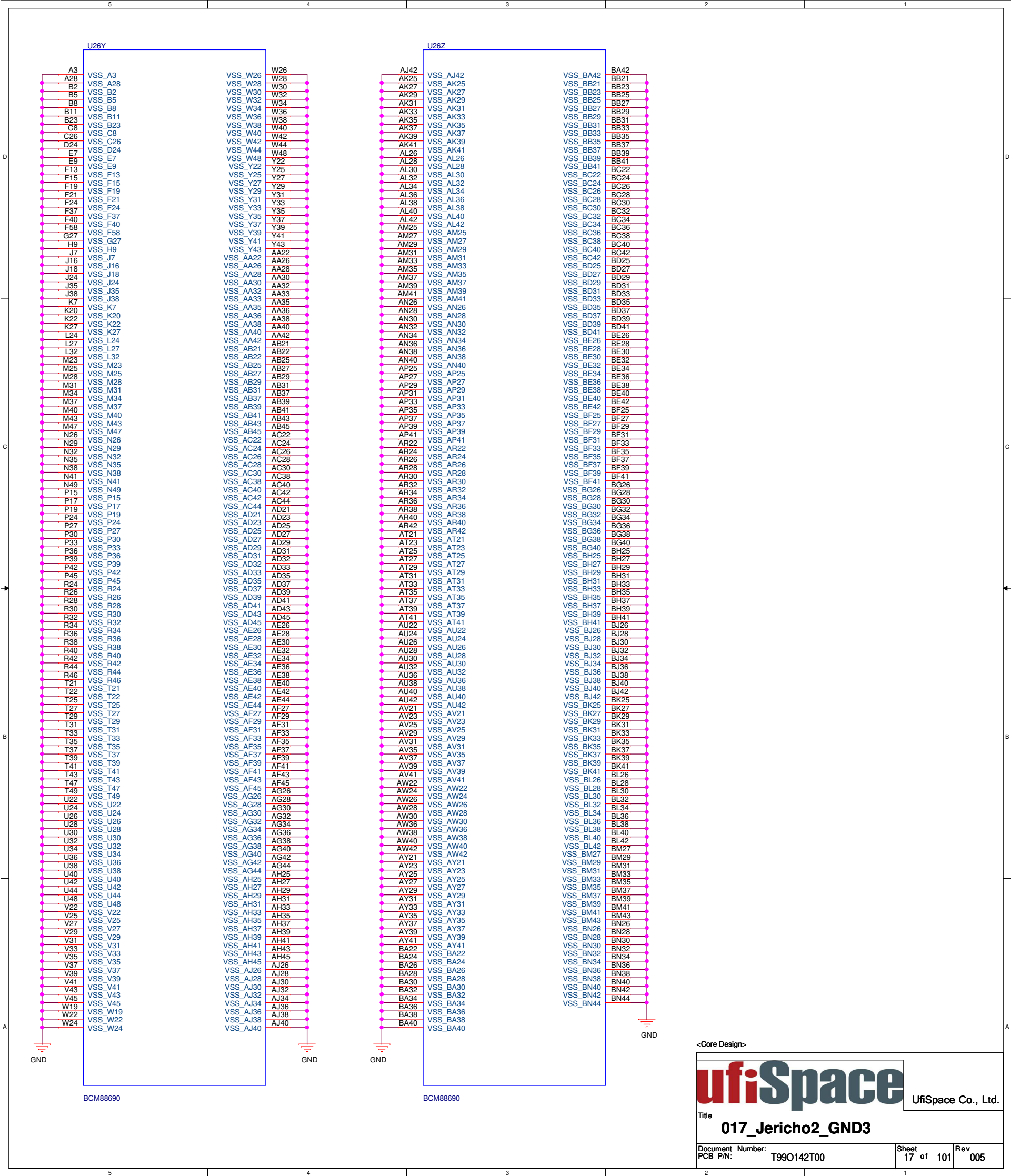


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UfiSpace Co., Ltd.

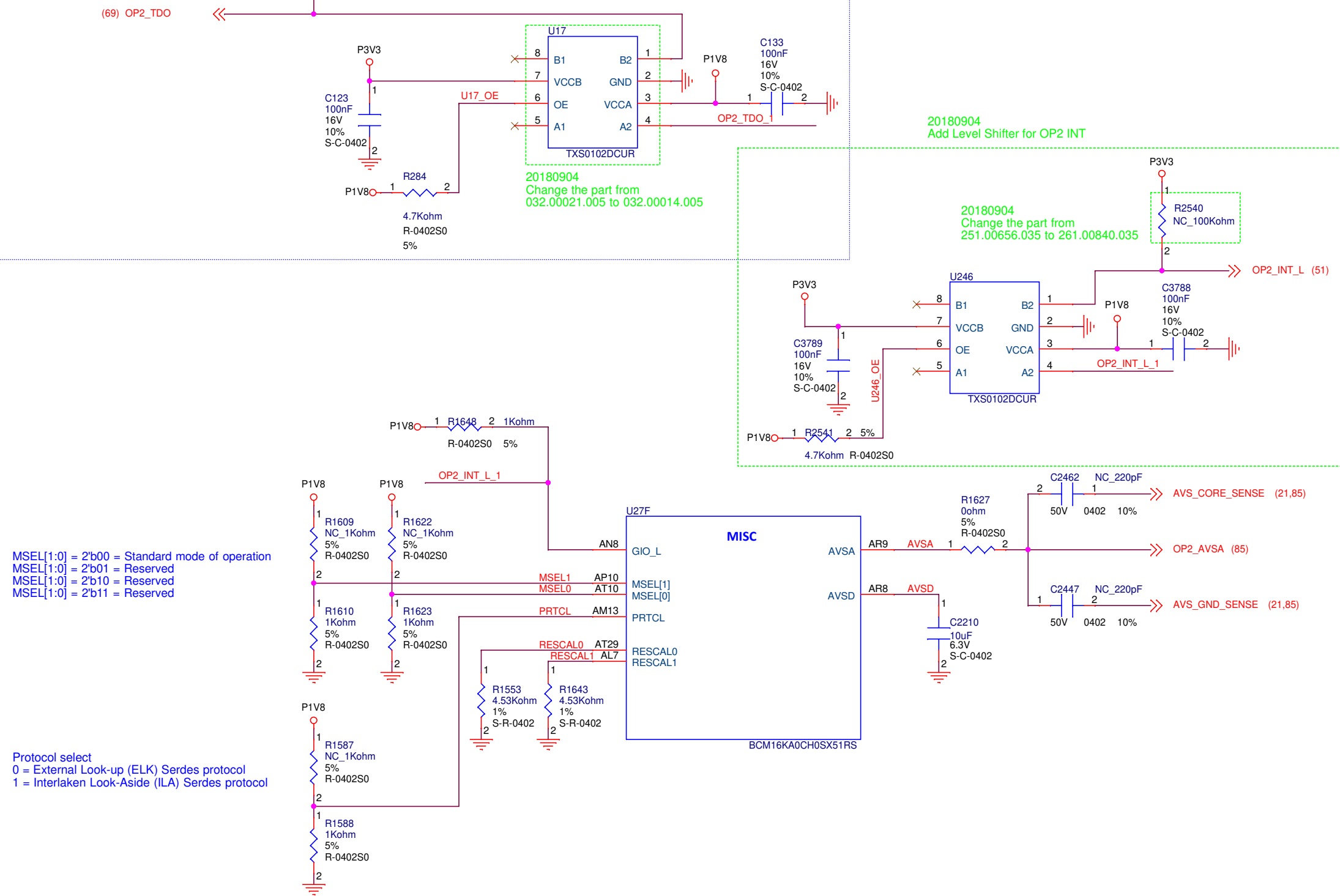
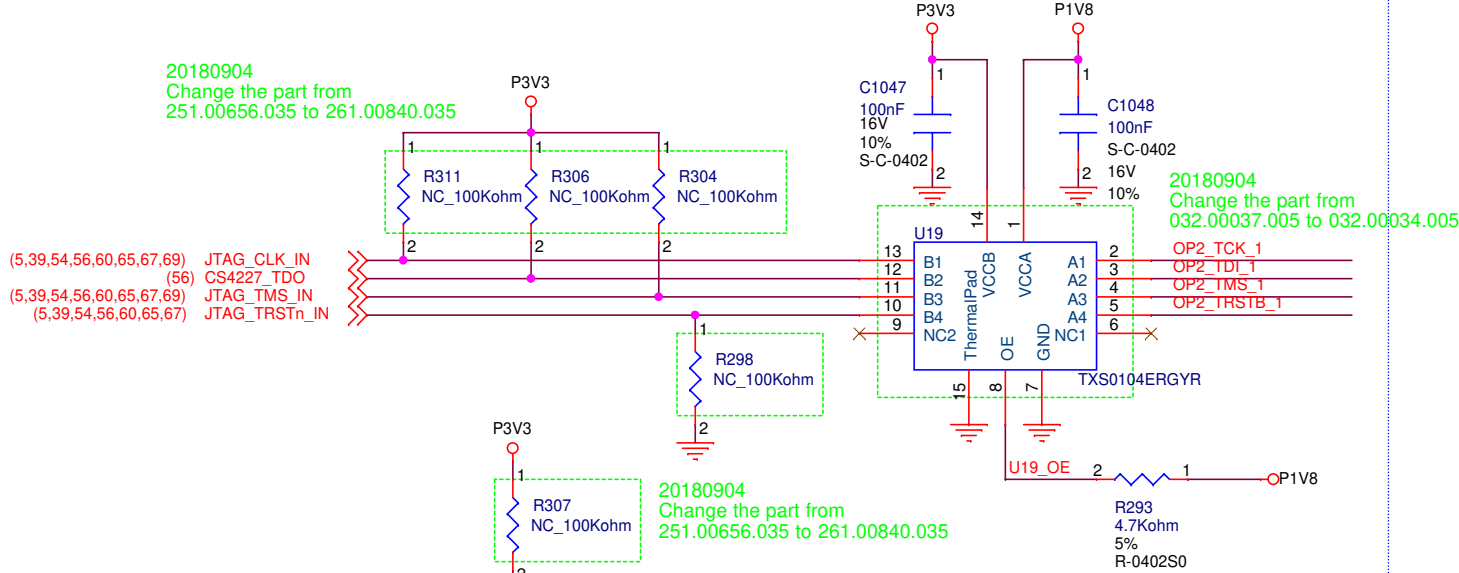
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017_Jericho2_GND3

Document Number:
PCB P/N: T99O142T00

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Rev
005

Level Shifter for JTAG Interface



FAB
8 Serdes @ 50Gbps

NIF
8 Serdes @ 50Gbps

FAB
8 Serdes @ 50Gbps

NIF
8 Serdes @ 50Gbps

Ingress Stats NIF

Egress Stats NIF

Ingress Stats NIF

Egress Stats NIF

<Core Design>

ufiSpace

UfiSpace Co., Ltd.

Title

019_OP2_Serdes

Document Number:
PCB P/N:

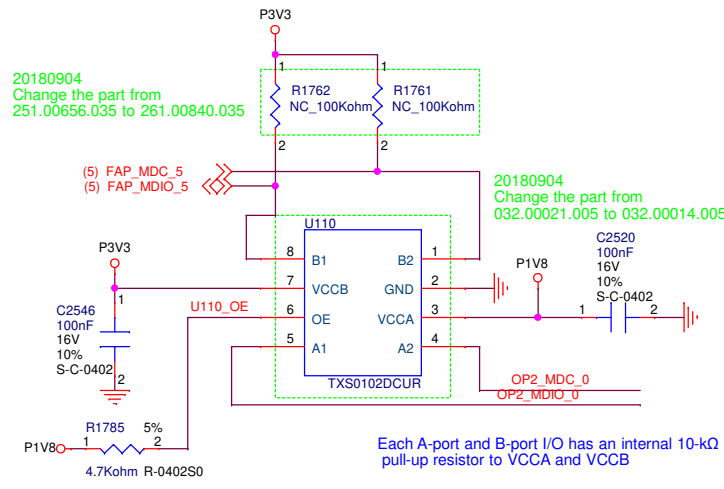
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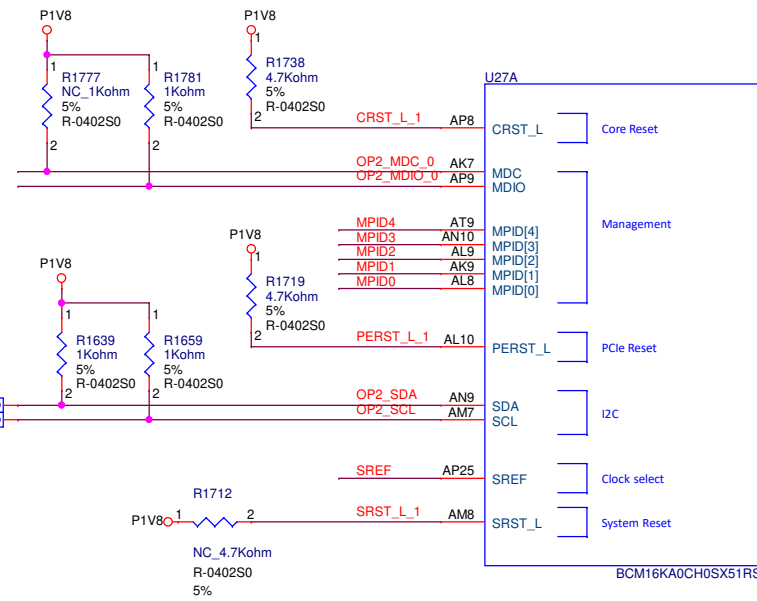
Rev
005

Level Shifter for MDC / MDIO

20180904
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251.00656.035 to 261.00840.035

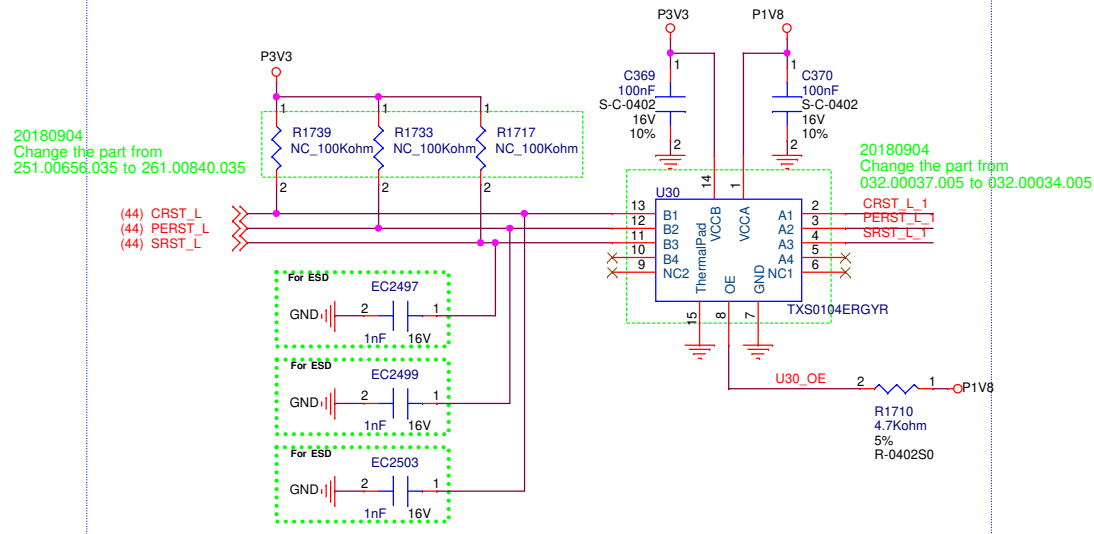


Each A-port and B-port I/O has an internal 10-kΩ pull-up resistor to VCCA and VCCB

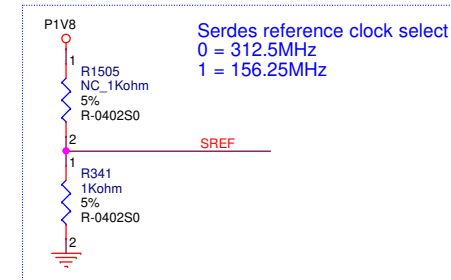
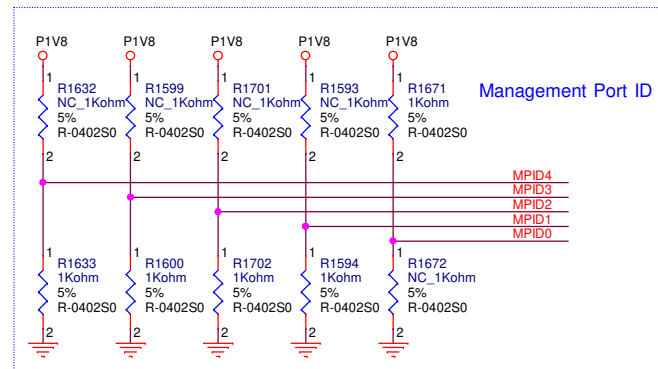


Level Shifter for Reset

20180904
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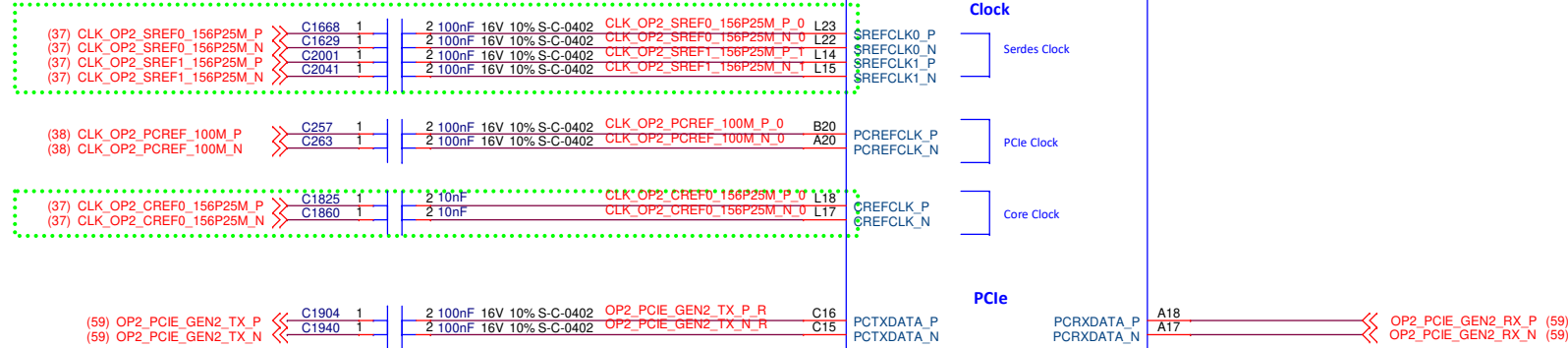
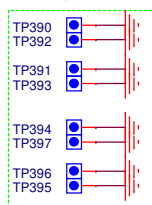


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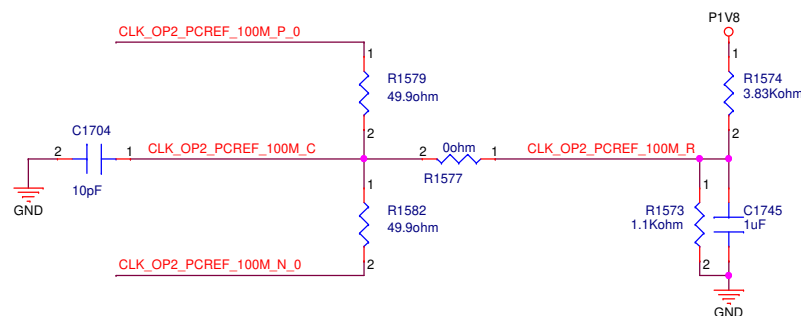


All reference clocks with internal termination of 100ohm resistor

20180904
Add GND test point to RMS Jitter measure



For the PCIe Rx pins, external AC-Coupling capacitors are required. The recommended value is 100nF.
For the chip receiving BCM16K PCIe Tx signals, it is required to have AC coupling (either built-in or on the board)



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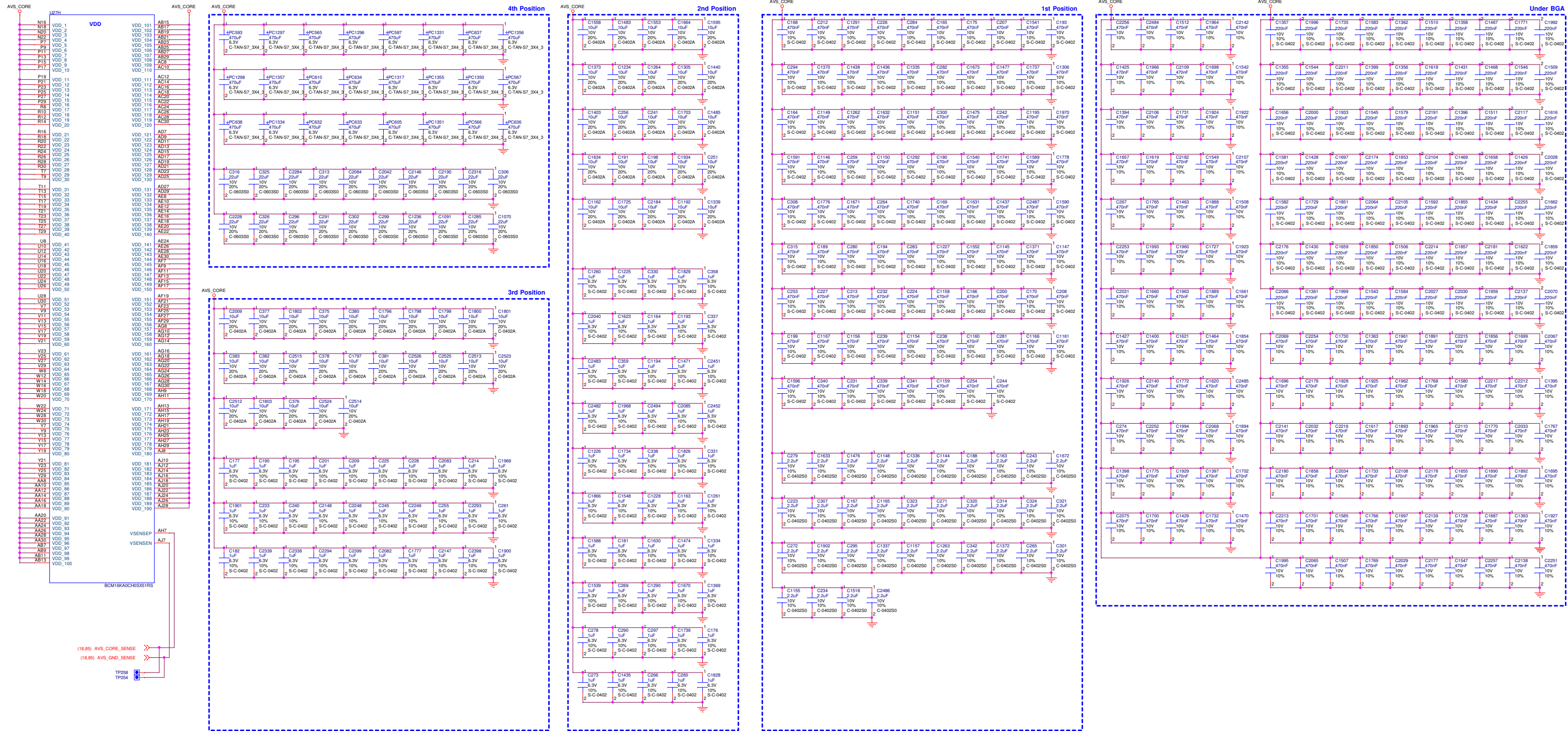
ufiSpace
UfiSpace Co., Ltd.

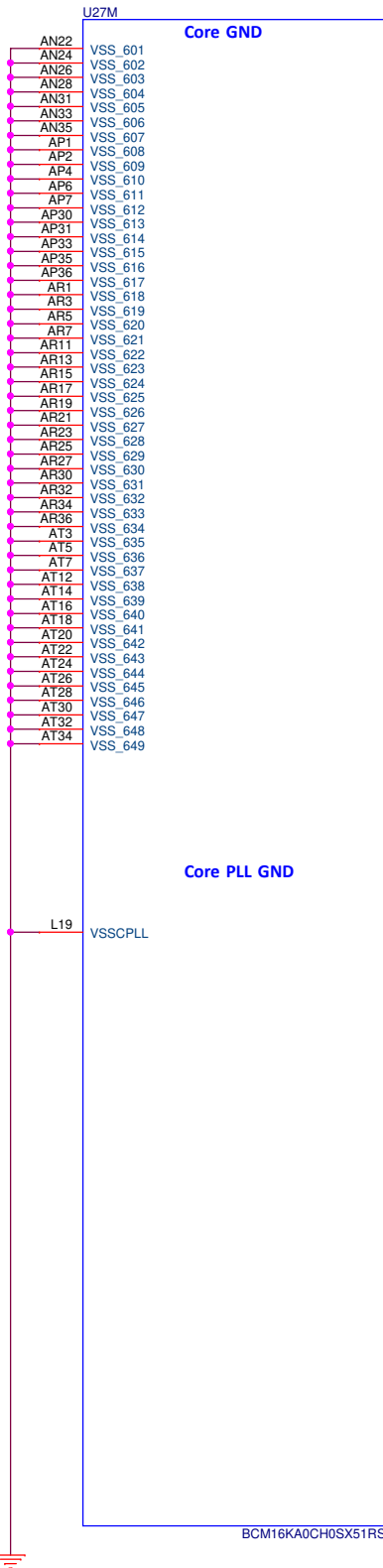
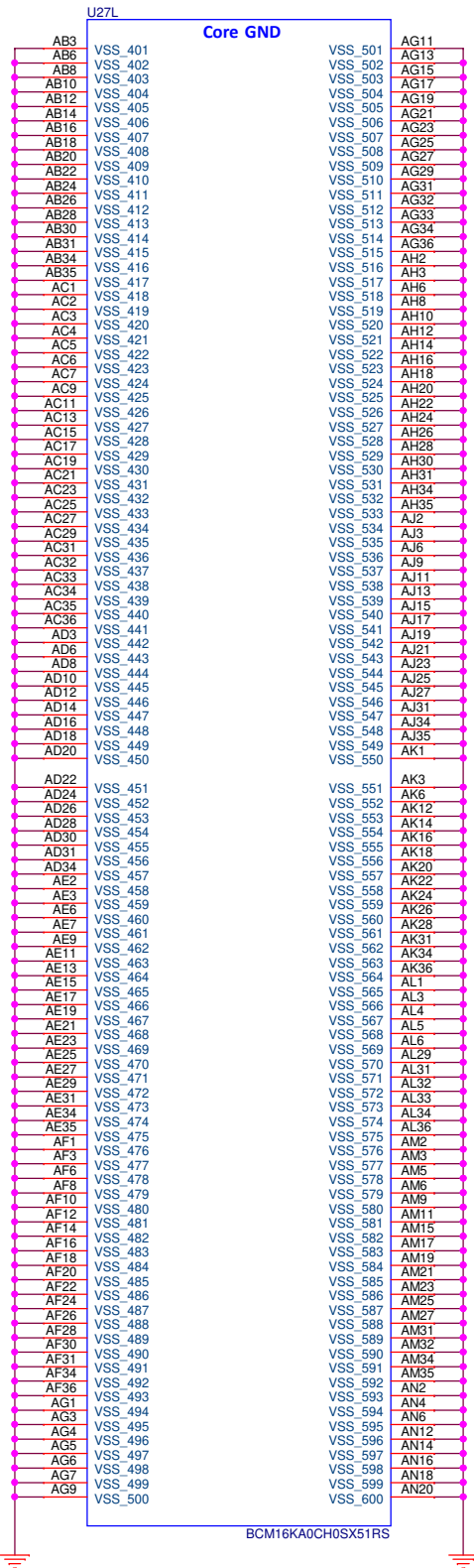
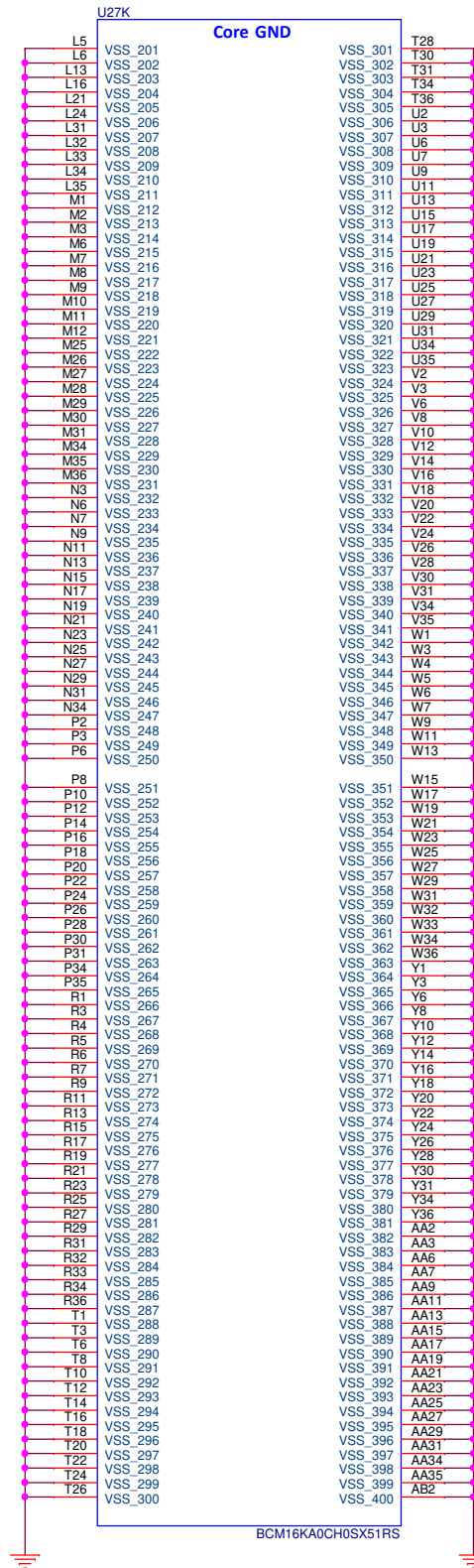
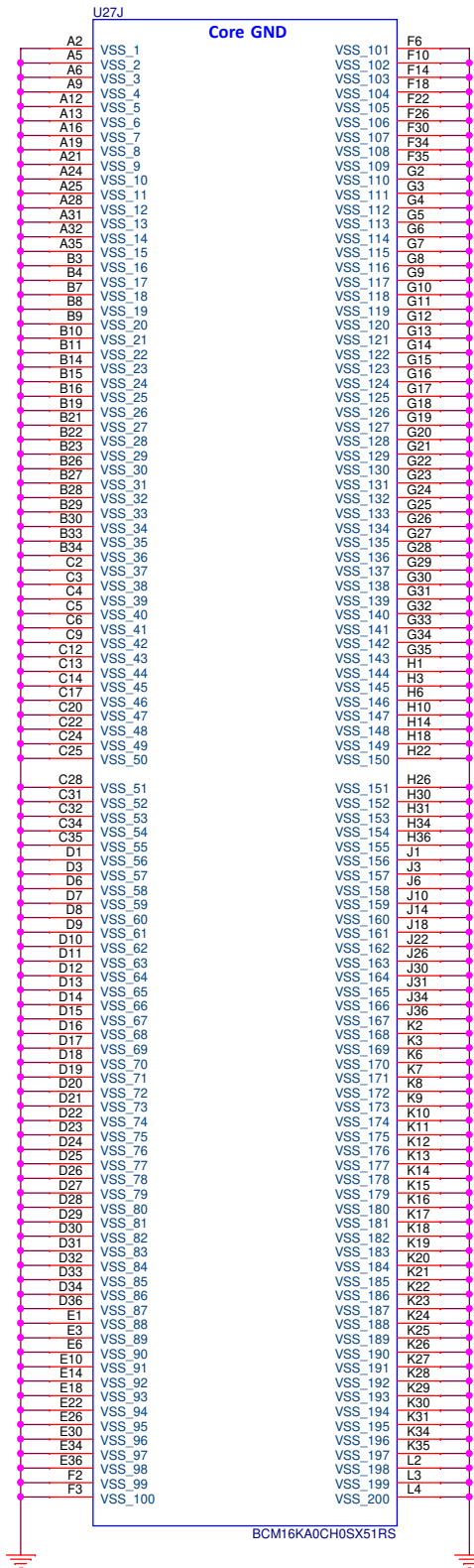
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Document Number:
PCB P/N: T99O142T00

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005





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Document Number:
PCB P/N: T99O142T00

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005

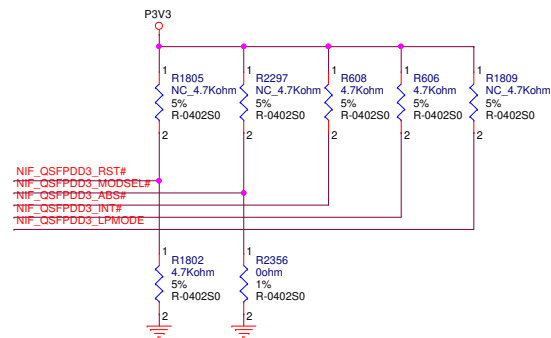
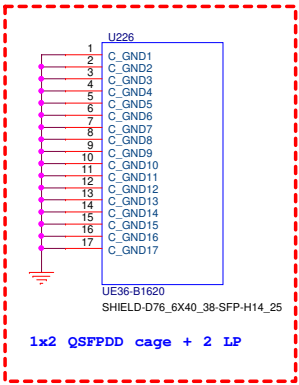
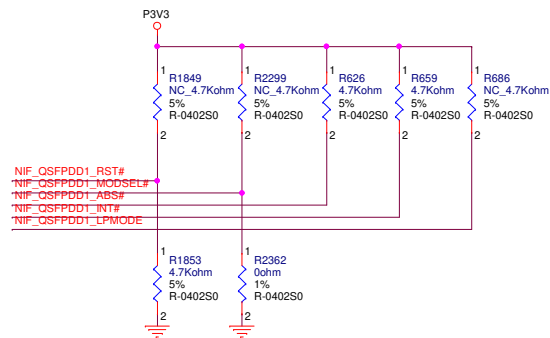
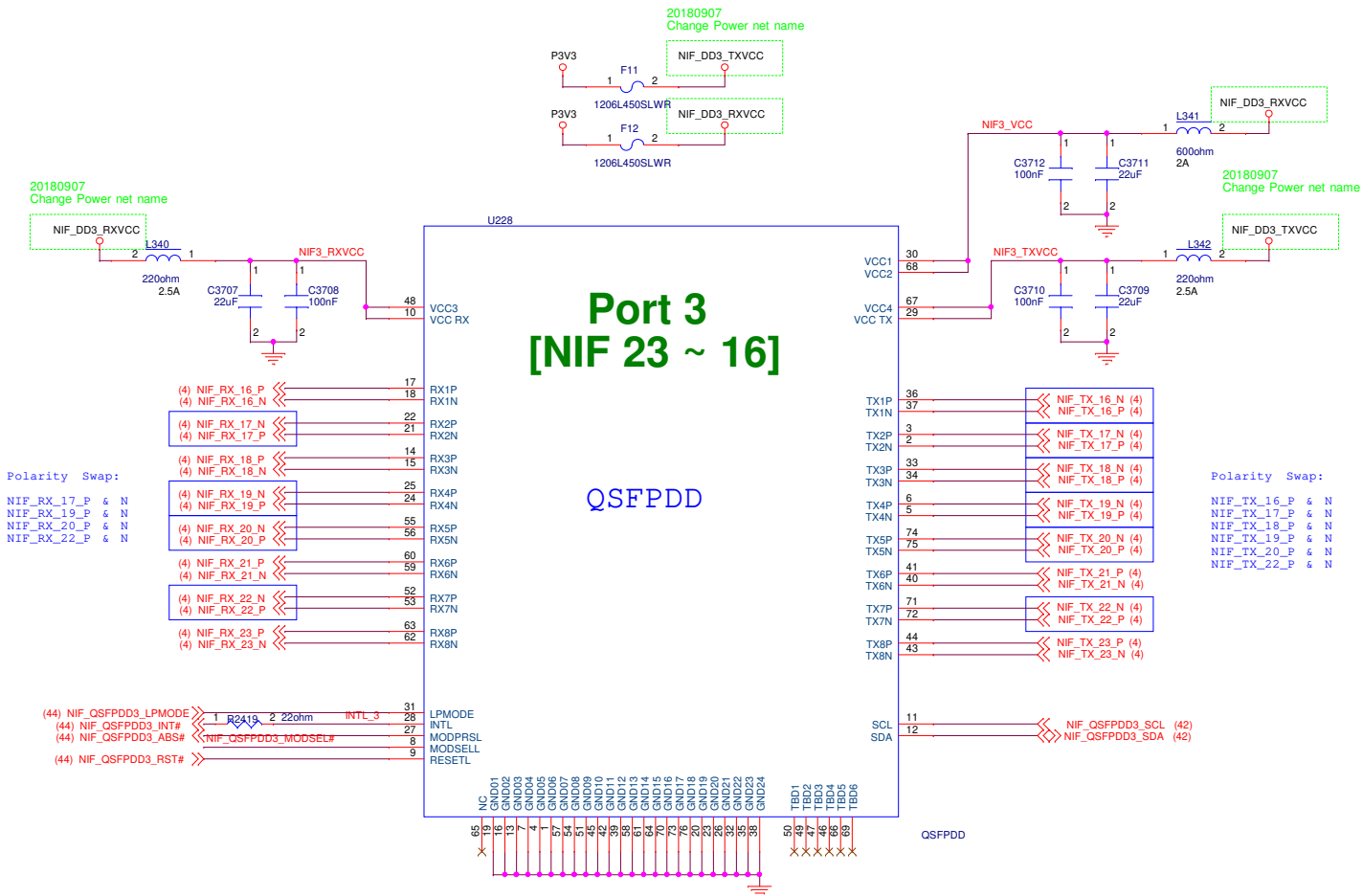
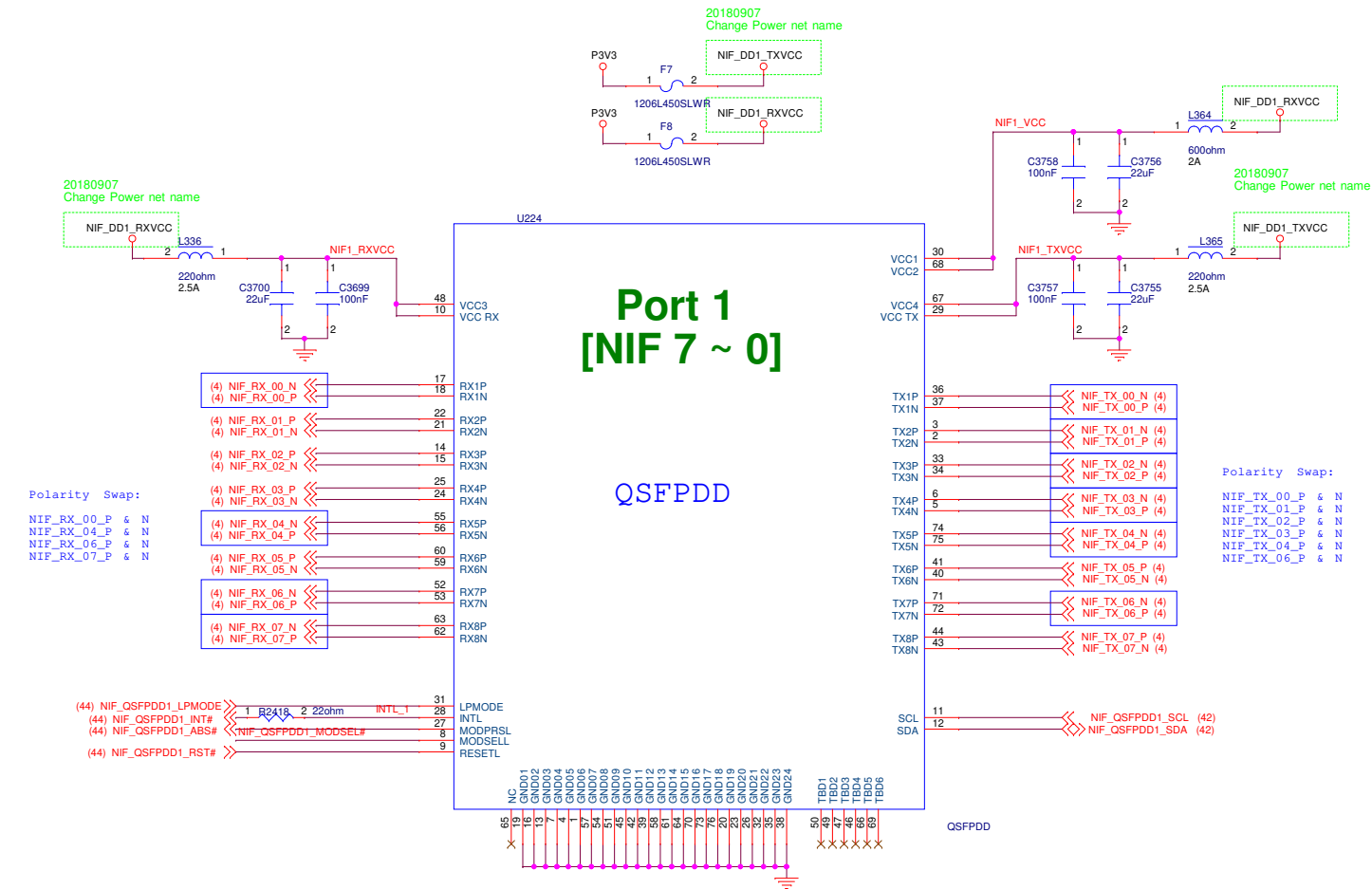
Blackhawk supports SerDes polarity inversion.

On the Blackhawk SerDes, there is no RX or TX mapping (swapping).

$\Delta \nabla$ $\Delta \nabla$ $\Delta \nabla$ $\Delta \nabla$ $\Delta \nabla$

The diagram illustrates a 5x5 network topology. The top row is labeled 'Lane #' and the bottom row is labeled 'Port #'. The columns are labeled with NIF ranges: [7:0], [23:16], [39:32], [95:88], and [79:72]. The middle row is labeled 'Port #'. The bottom row is labeled 'Port #'. The NIF ranges are: [7:0], [23:16], [39:32], [95:88], and [79:72]. The Port # labels are: Port 1, Port 3, Port 5, Port 7, and Port 9. The NIF ranges are: [15:8], [31:24], [47:40], [87:80], and [71:64]. The Port # labels are: Port 2, Port 4, Port 6, Port 8, and Port 10.

Lane #	NIF [7:0]	NIF [23:16]	NIF [39:32]	NIF [95:88]	NIF [79:72]
Port #	Port 1	Port 3	Port 5	Port 7	Port 9
Port #	Port 2	Port 4	Port 6	Port 8	Port 10



2.3 Blackhawk P/N Polarity Inversion

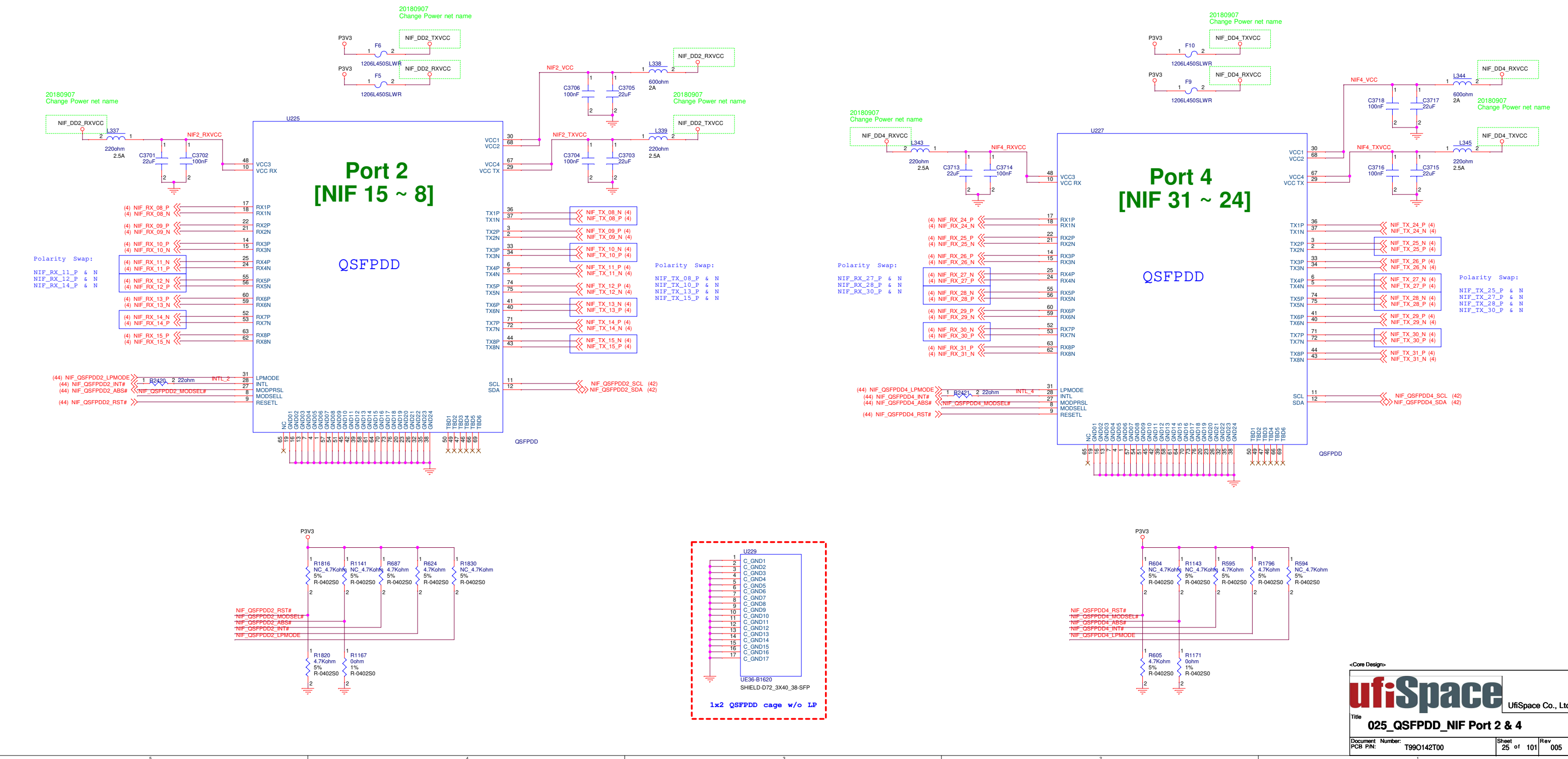
Blackhawk supports SerDes polarity inversion.

2.4.2 Blackhawk Lane Mapping – NIF Ethernet

On the Blackhawk SerDes, there is no RX or TX mapping (swapping).

NIF Port Mapping

	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽
Lane #	NIF [7:0]	NIF [23:16]	NIF [39:32]	NIF [95:88]	NIF [79:72]
Lane #	NIF [15:8]	NIF [31:24]	NIF [47:40]	NIF [87:80]	NIF [71:64]
Port #	Port 1	Port 3	Port 5	Port 7	Port 9
Port #	Port 2	Port 4	Port 6	Port 8	Port 10



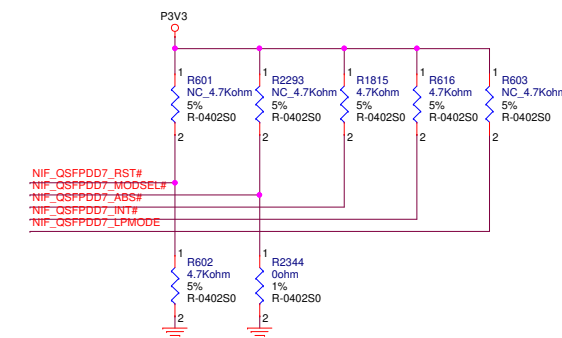
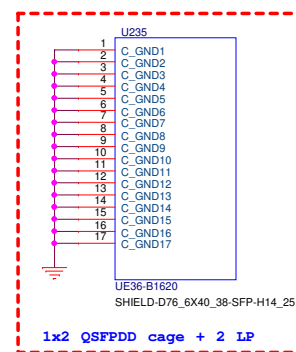
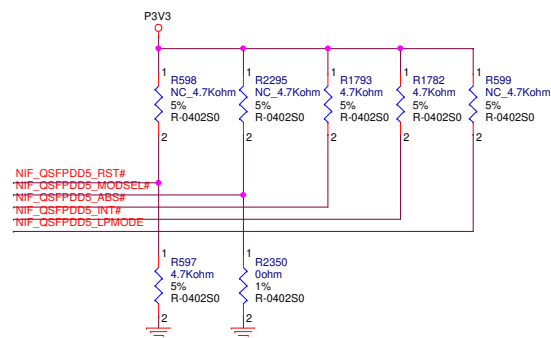
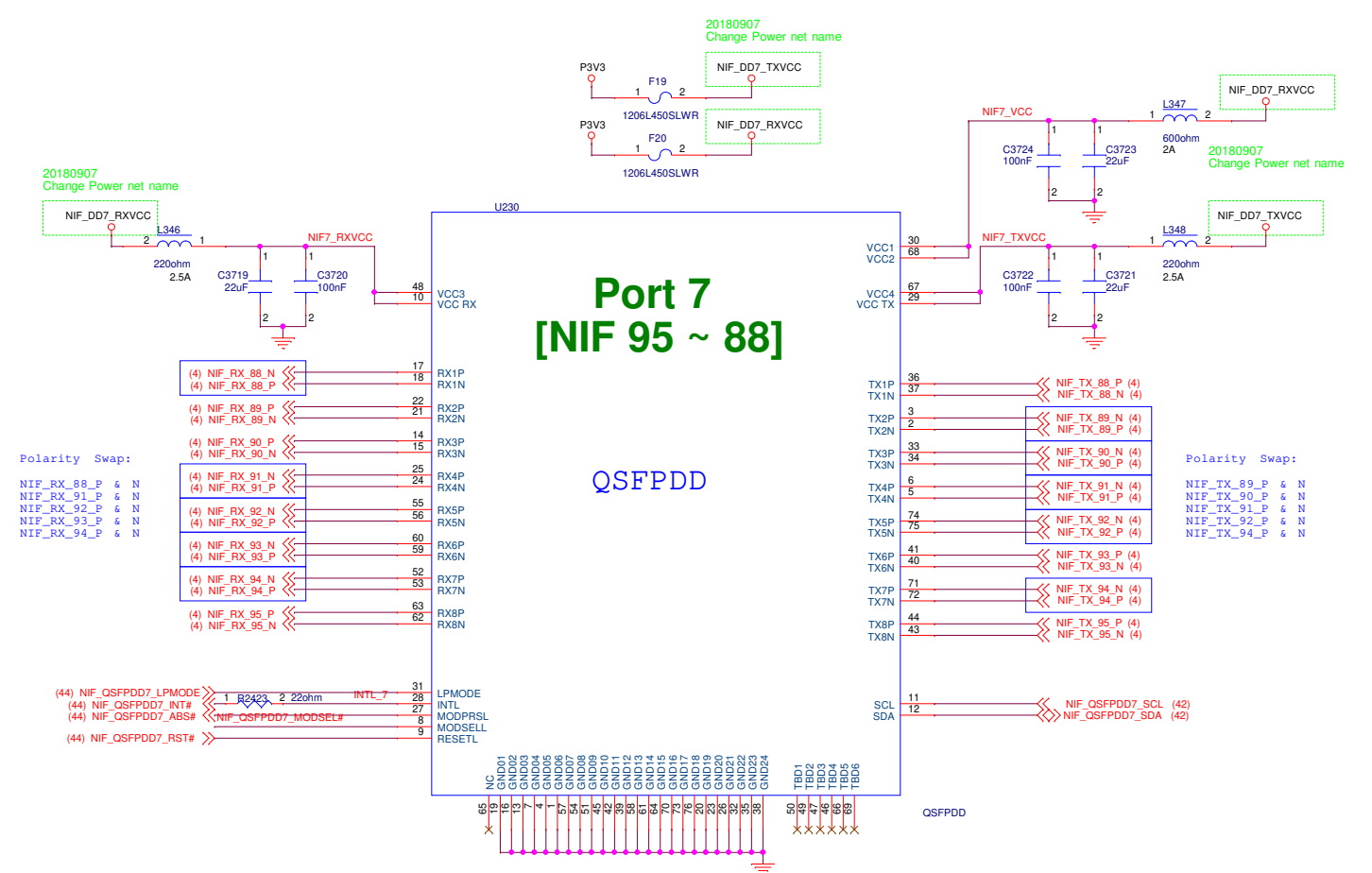
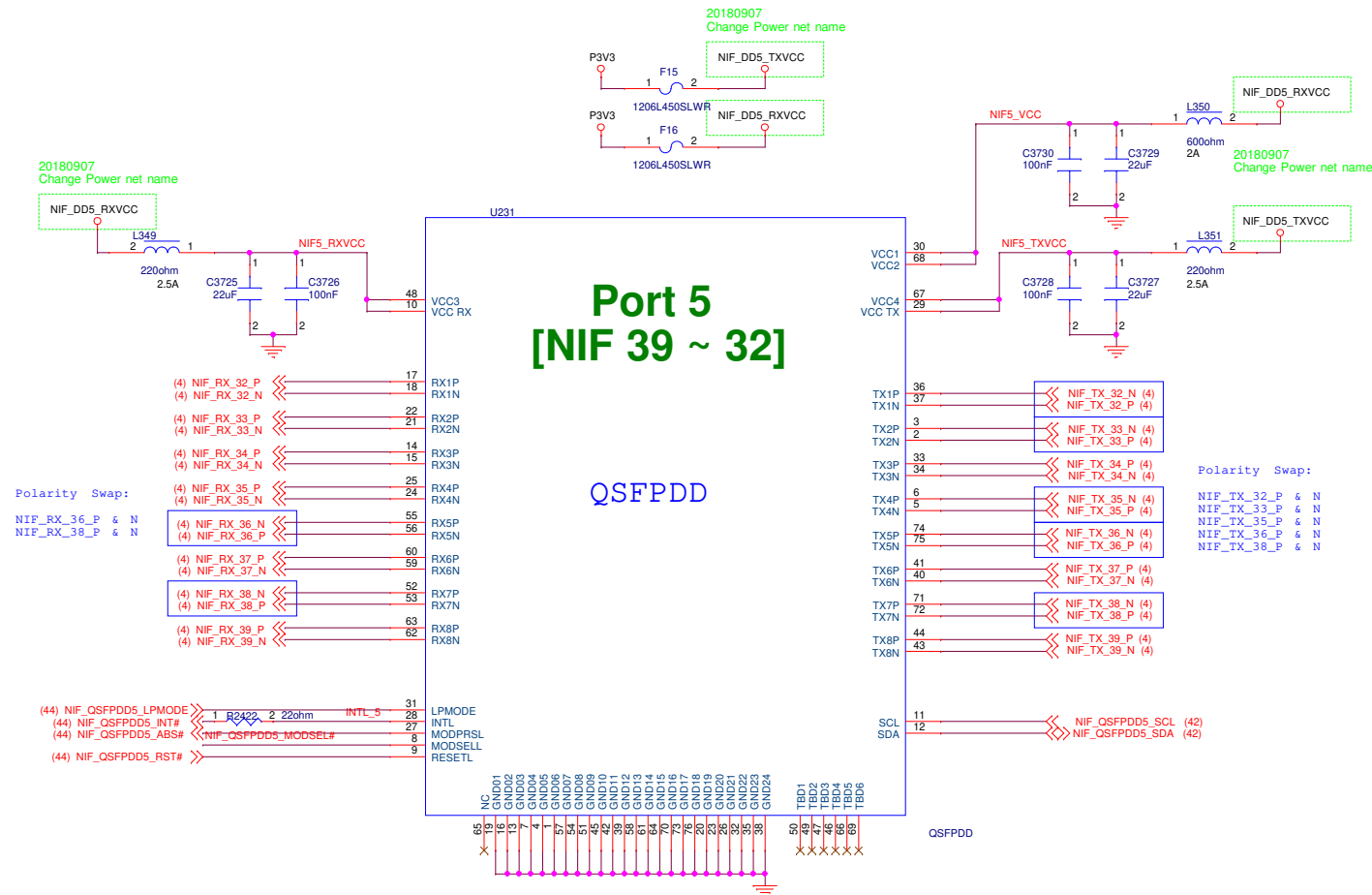
Blackhawk supports SerDes polarity inversion.

2.4.2 Blackhawk Lane Mapping – NIF Ethernet

On the Blackhawk SerDes, there is no RX or TX mapping (swapping).

NIF Port Mapping

	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
Lane #	NIF [7:0]	NIF [23:16]	NIF [39:32]	NIF [95:88]	NIF [79:72]
Lane #	NIF [15:8]	NIF [31:24]	NIF [47:40]	NIF [87:80]	NIF [71:64]
	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
Port #	Port 1	Port 3	Port 5	Port 7	Port 9
Port #	Port 2	Port 4	Port 6	Port 8	Port 10



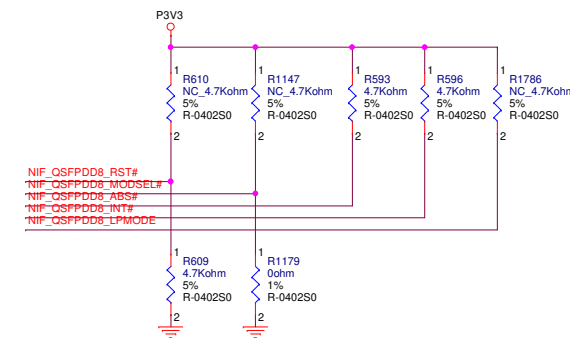
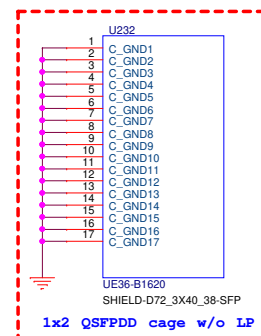
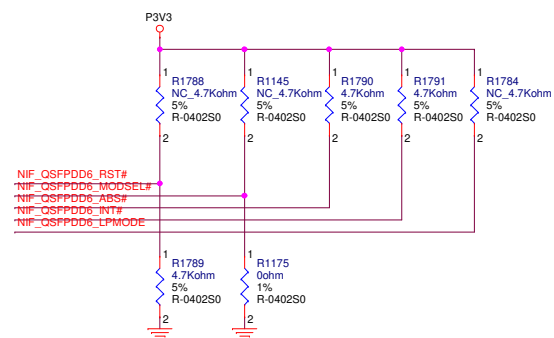
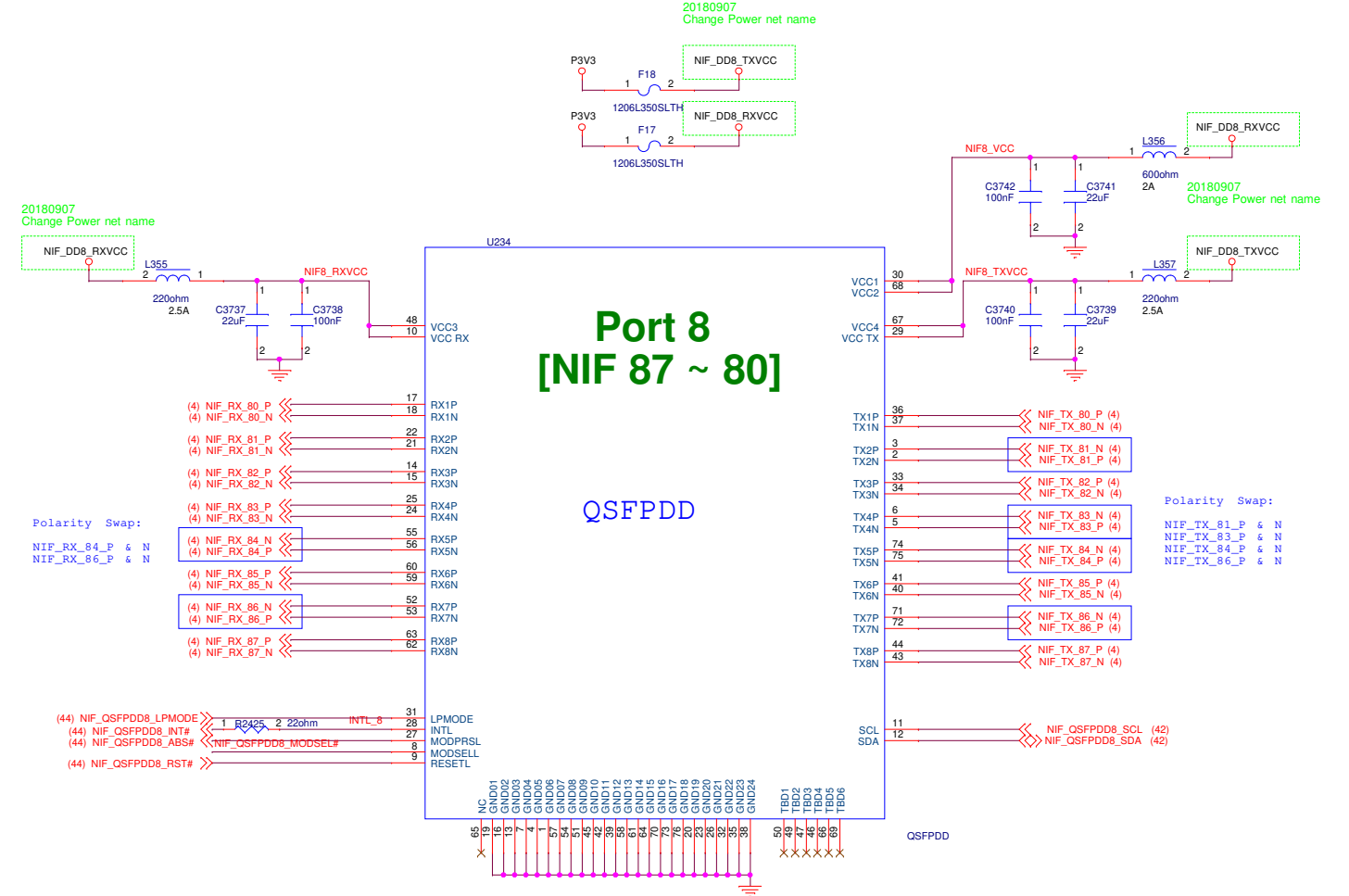
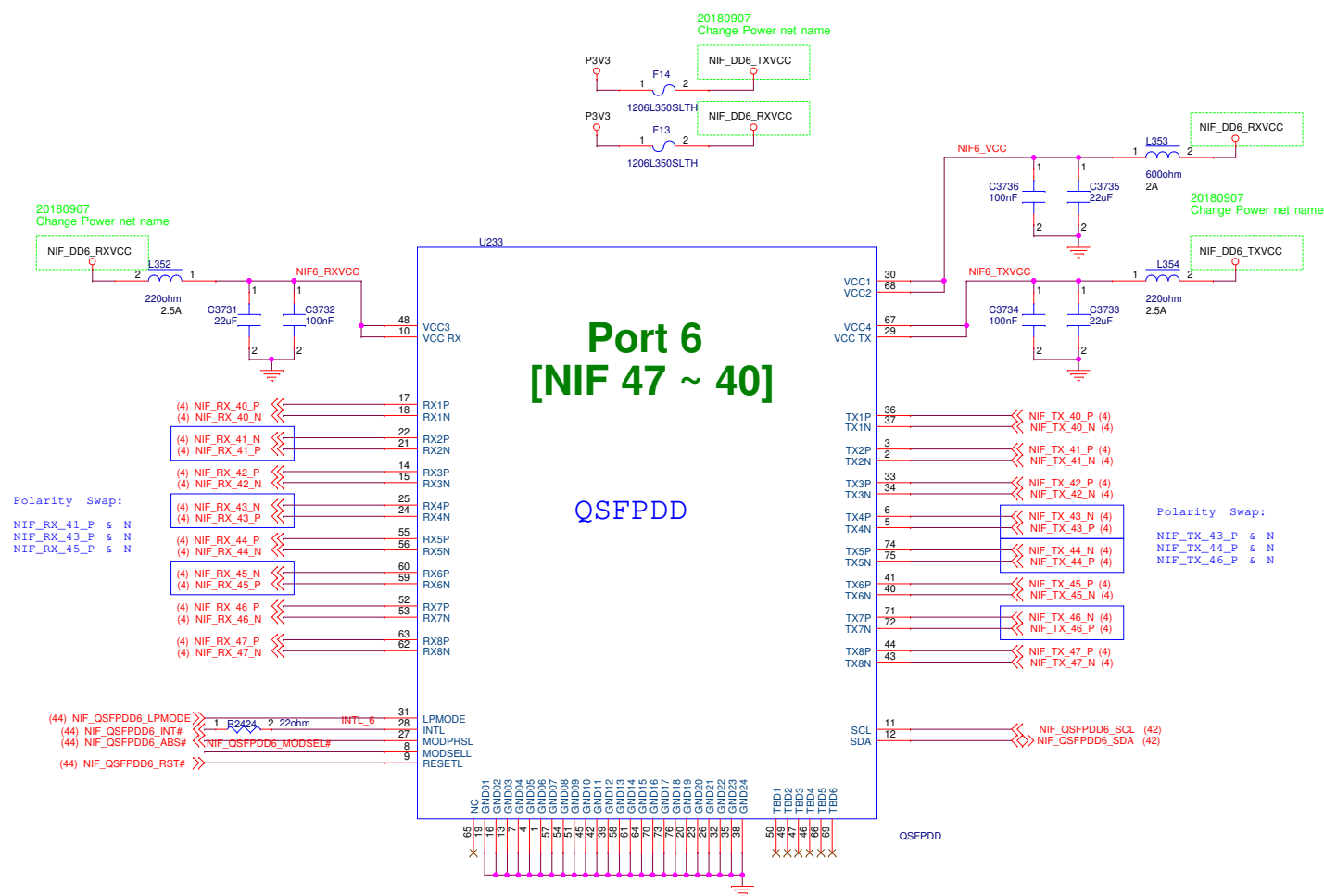
Blackhawk supports SerDes polarity inversion.

2.4.2 Blackhawk Lane Mapping – NIF Ethernet

On the Blackhawk SerDes, there is no RX or TX mapping (swapping).

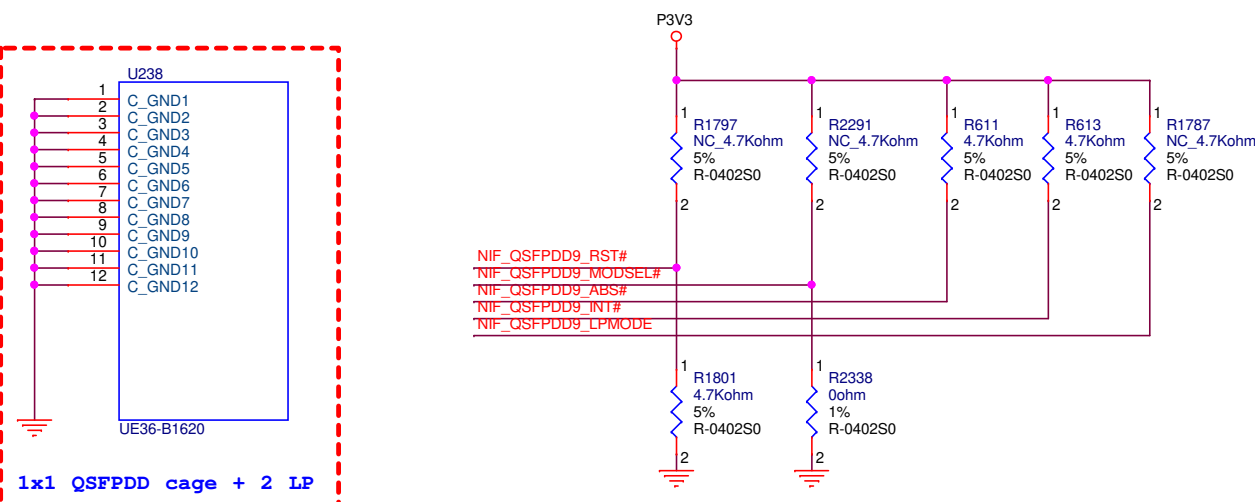
NIF Port Mapping

	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
Lane #	NIF [7:0]	NIF [23:16]	NIF [39:32]	NIF [95:88]	NIF [79:72]
Lane #	NIF [15:8]	NIF [31:24]	NIF [47:40]	NIF [87:80]	NIF [71:64]
	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
Port #	Port 1	Port 3	Port 5	Port 7	Port 9
Port #	Port 2	Port 4	Port 6	Port 8	Port 10



Blackhawk supports SerDes polarity inversion.

On the Blackhawk SerDes, there is no RX or TX mapping (swapping).

[illegible]

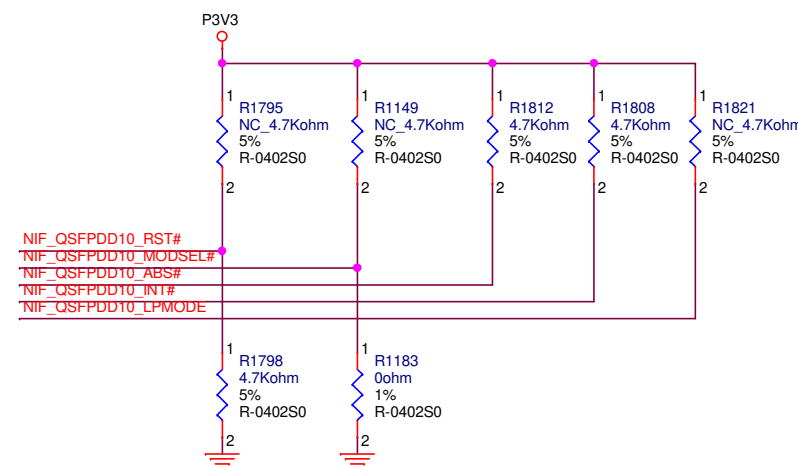
Blackhawk supports SerDes polarity inversion.

On the Blackhawk SerDes, there is no RX or TX mapping (swapping).



Diagram of a 1x1 QSFPDD cage with 2 LP. The component is labeled U239 and UE36-B1620. The pins are numbered 1 through 12. The connections are as follows:

- Pin 1: C_GND1
- Pin 2: C_GND2
- Pin 3: C_GND3
- Pin 4: C_GND4
- Pin 5: C_GND5
- Pin 6: C_GND6
- Pin 7: C_GND7
- Pin 8: C_GND8
- Pin 9: C_GND9
- Pin 10: C_GND10
- Pin 11: C_GND11
- Pin 12: C_GND12



Blackhawk supports SerDes polarity inversion.

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

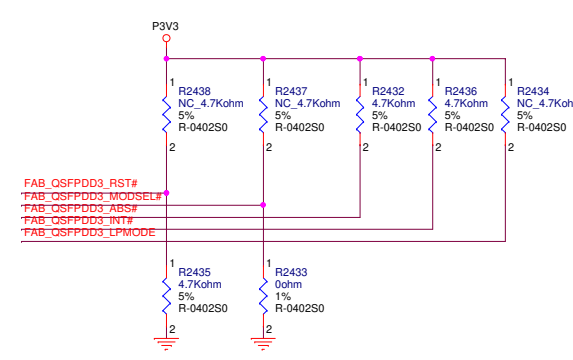
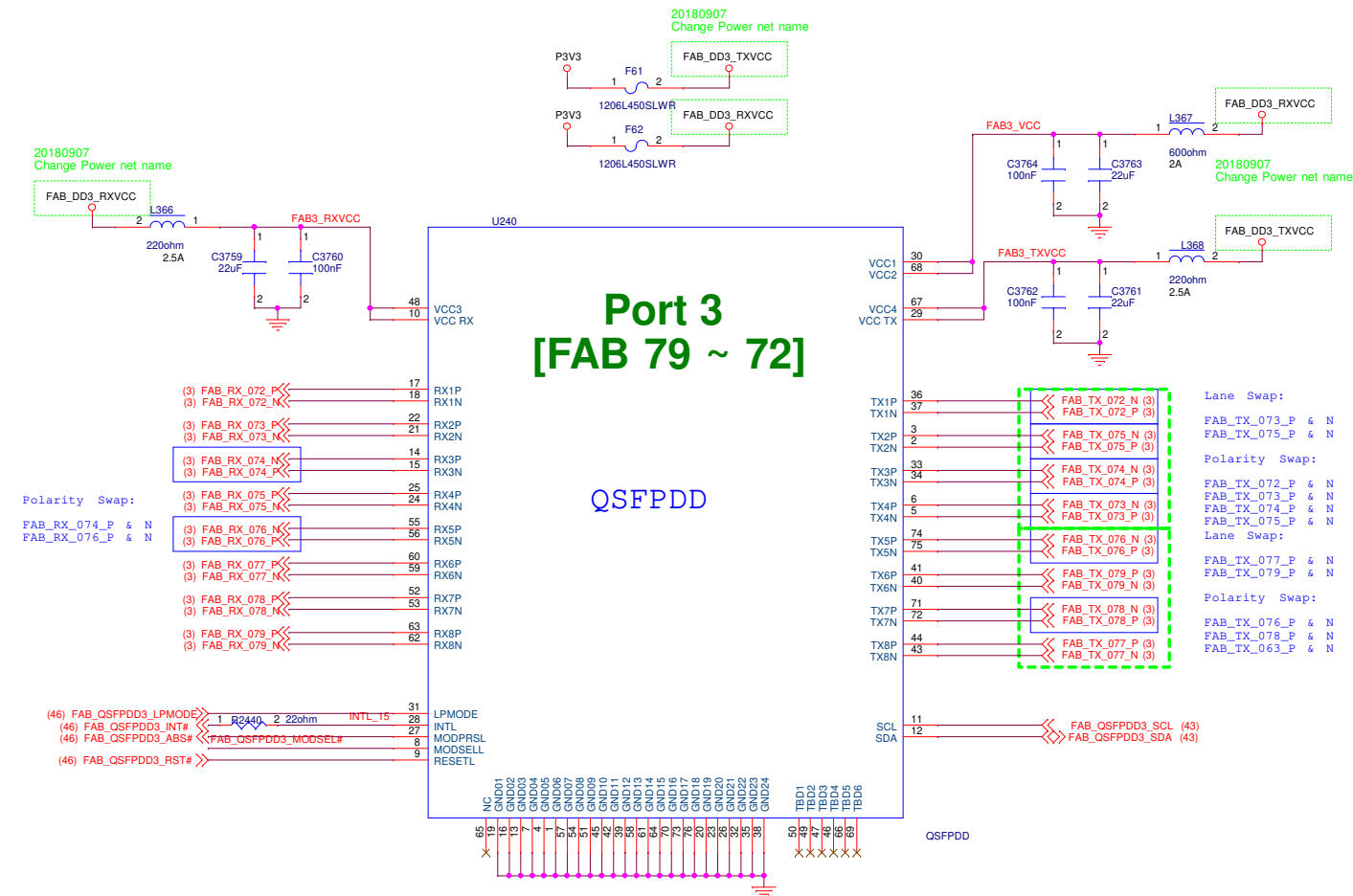
The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]

$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	

$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13

$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$	$\Delta \nabla$
Port 2	Port 4	Port 6	Port 8	Port 10	Port 12

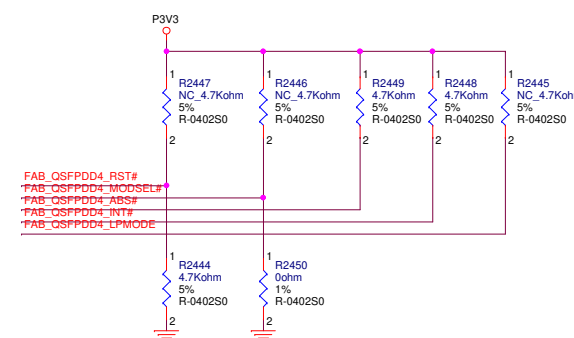
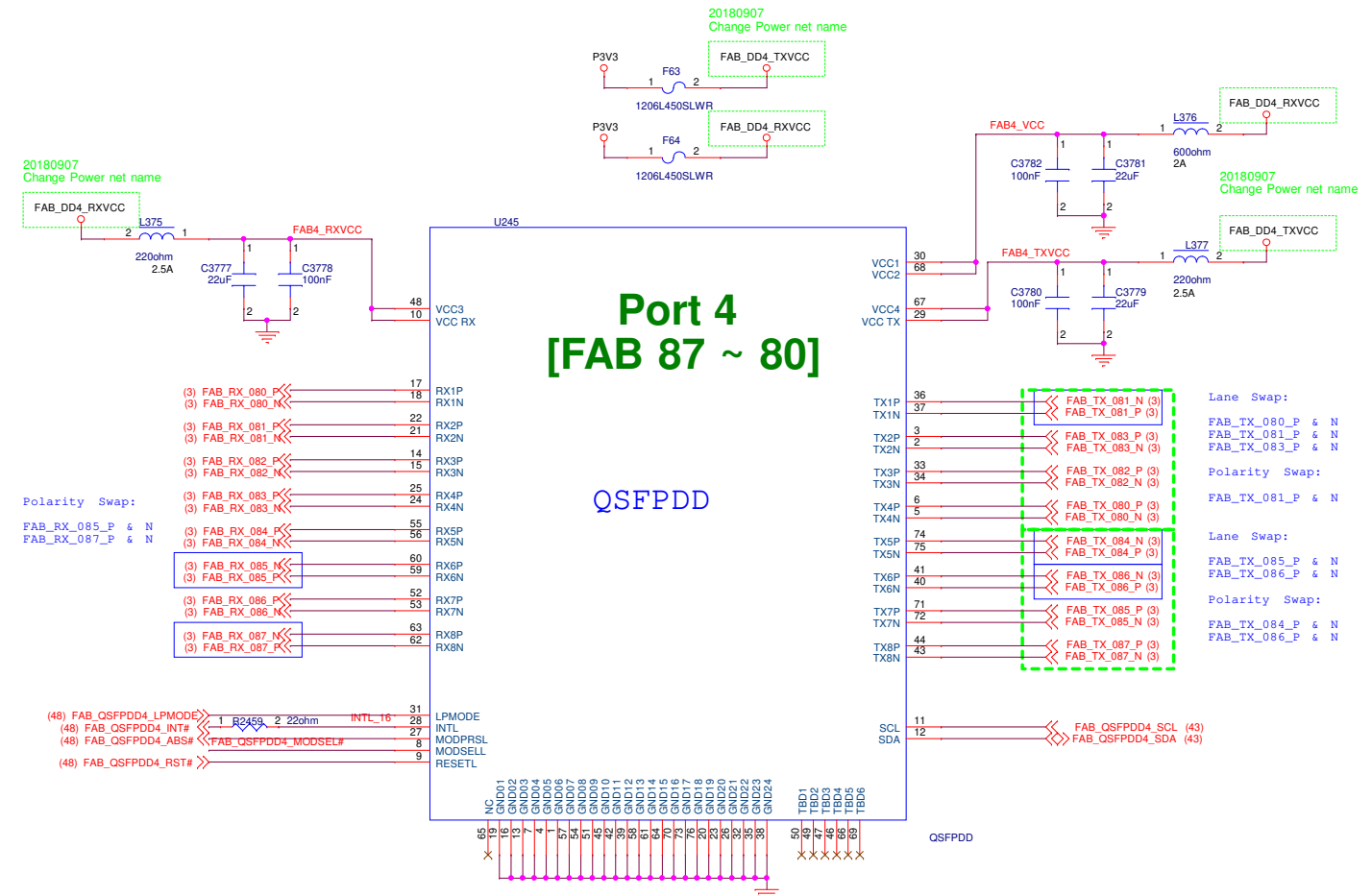


Blackhawk supports SerDes polarity inversion.

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽
Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	



2.3 Blackhawk P/N Polarity Inversion

Blackhawk supports SerDes polarity inversion.

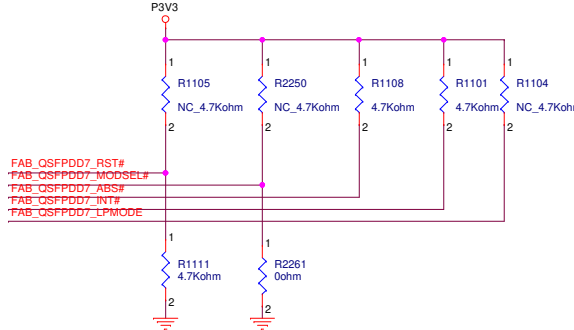
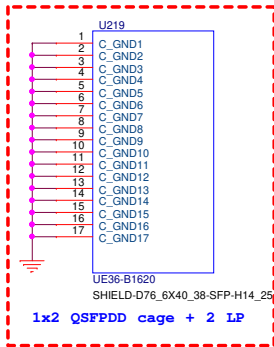
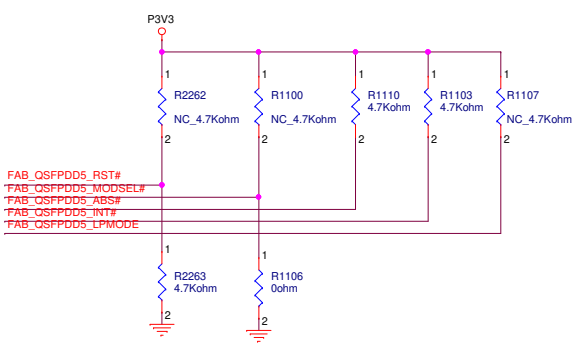
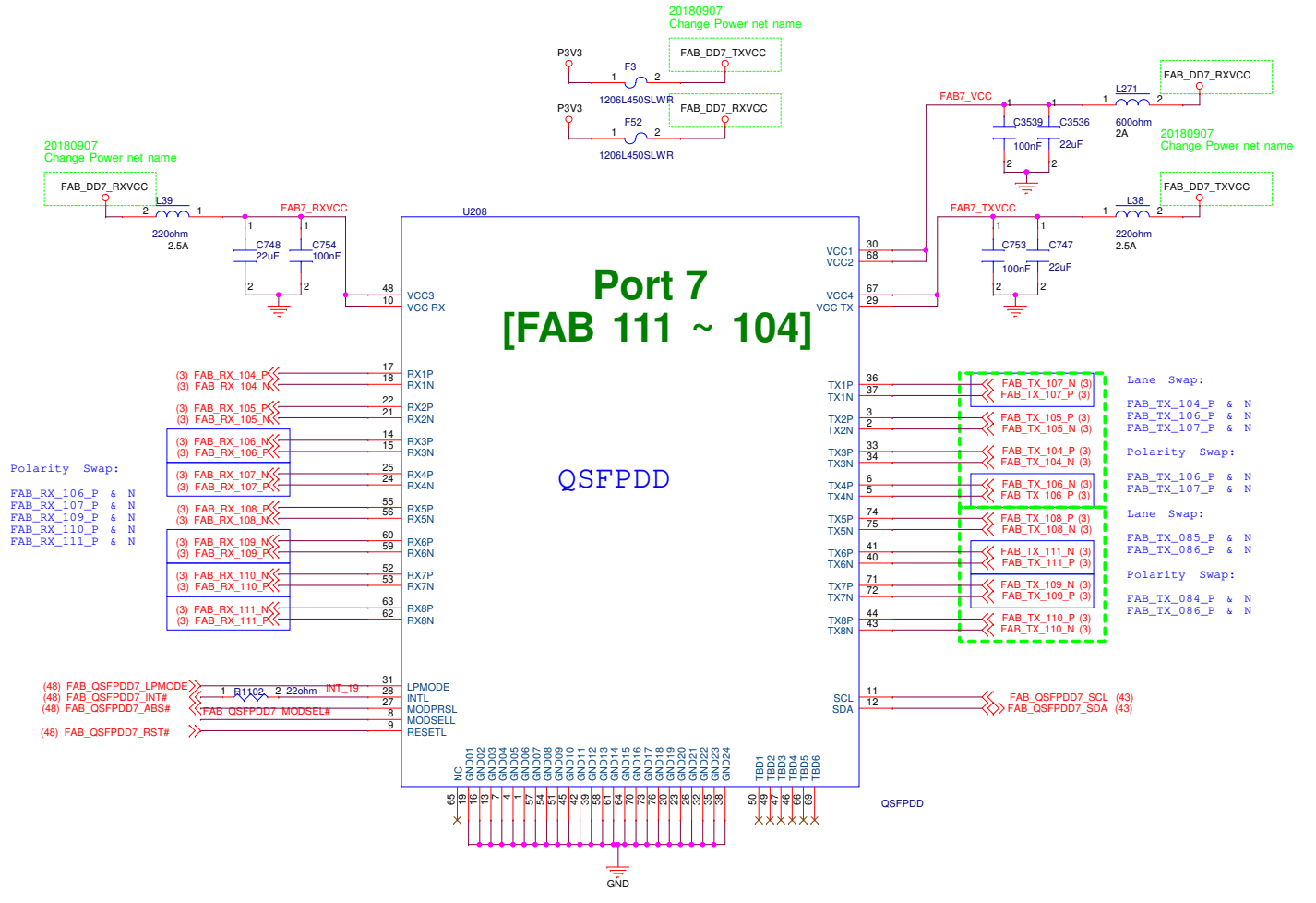
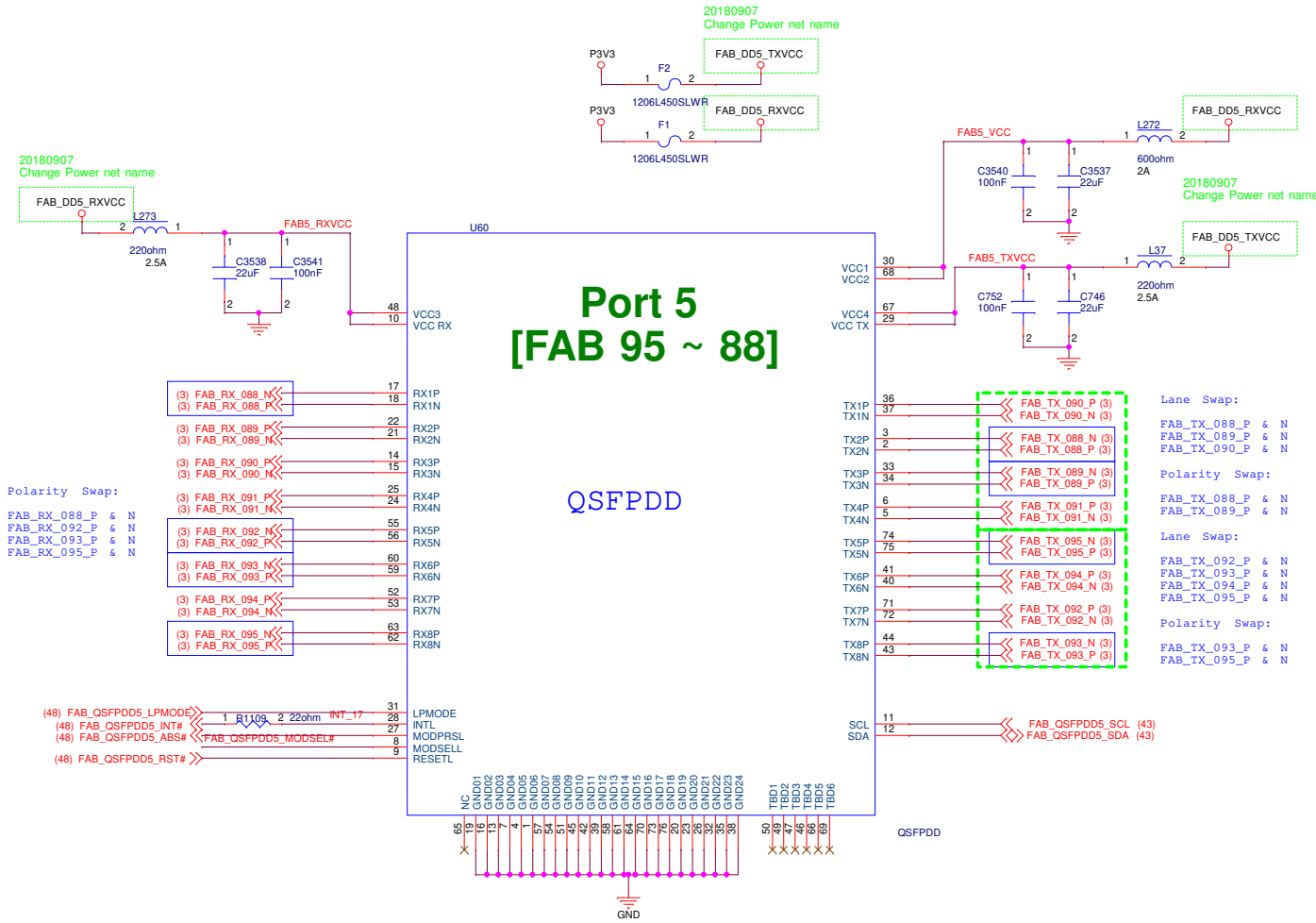
2.4.1 Blackhawk Lane Mapping – Fabric

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

The term quad is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

FAB Port Mapping

Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	

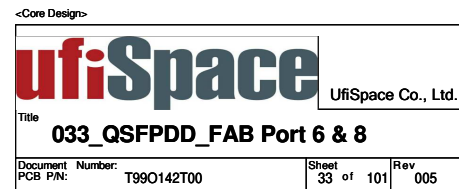


Blackhawk supports SerDes polarity inversion.

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

The term *quad* is used throughout this section to refer to a set of four RX/TX pairs. Two quads form the Blackhawk SerDes octet, which supports eight lanes. In each Blackhawk SerDes block, lanes 0–3 belong to one quad, and lanes 4–7 belong to the other quad.

	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	
Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	



Blackhawk supports SerDes polarity inversion.

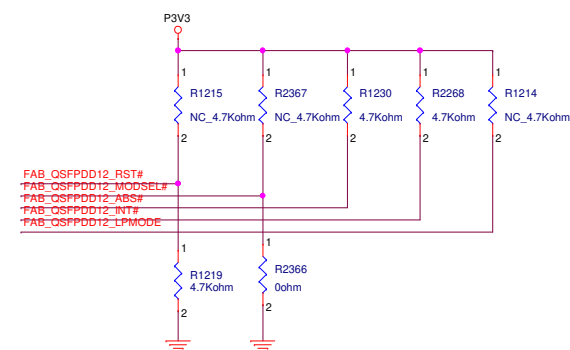
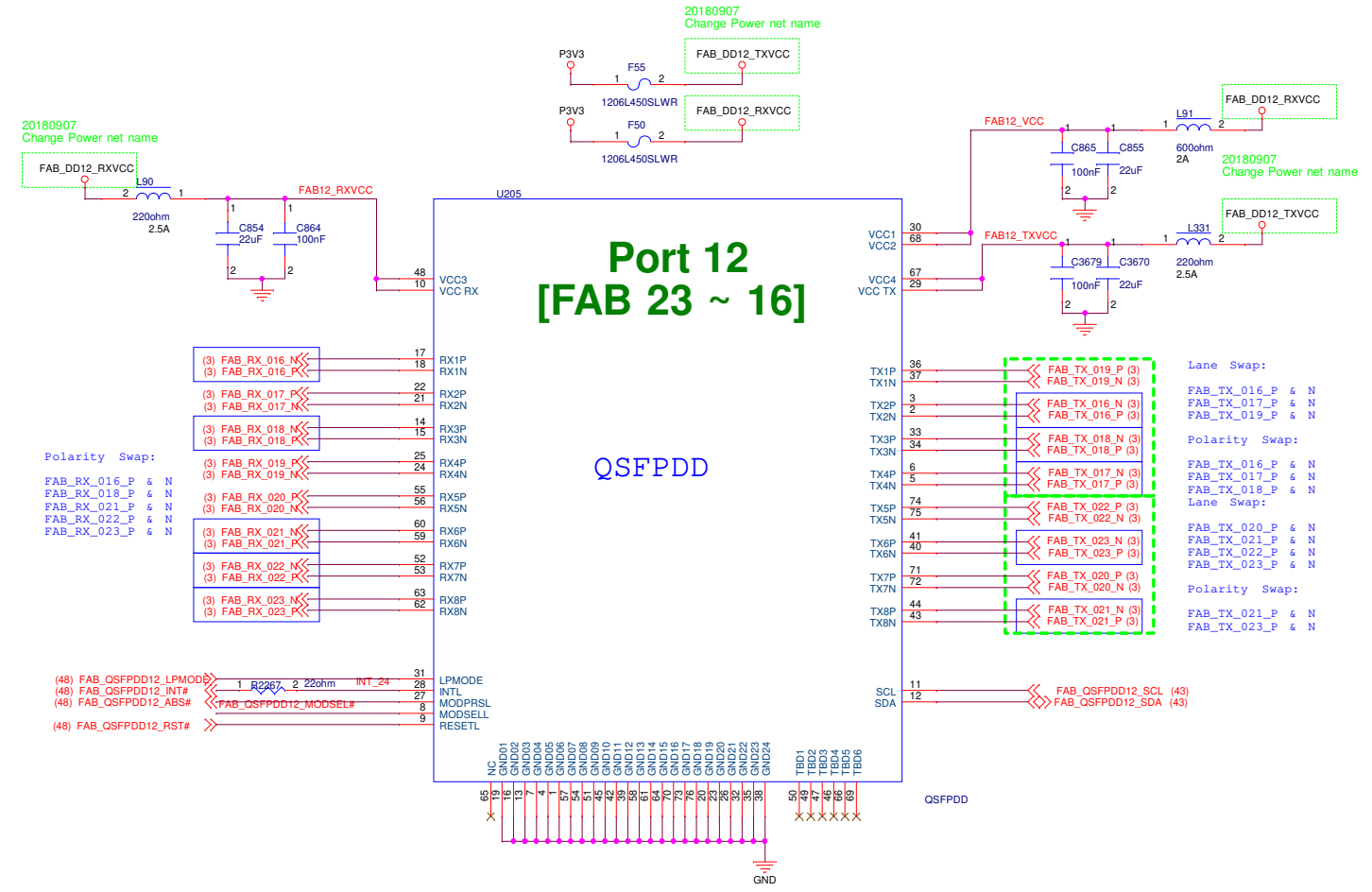
Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

Blackhawk supports SerDes polarity inversion.

Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.

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	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	
Lane #	FAB [63:56]	FAB [79:72]	FAB [95:88]	FAB [111:104]	FAB [47:40]	FAB [31:24]	FAB [15:8]
Lane #	FAB [71:64]	FAB [87:80]	FAB [103:96]	FAB [55:48]	FAB [39:32]	FAB [23:16]	
	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽	△ ▽
Port #	Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13
Port #	Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	

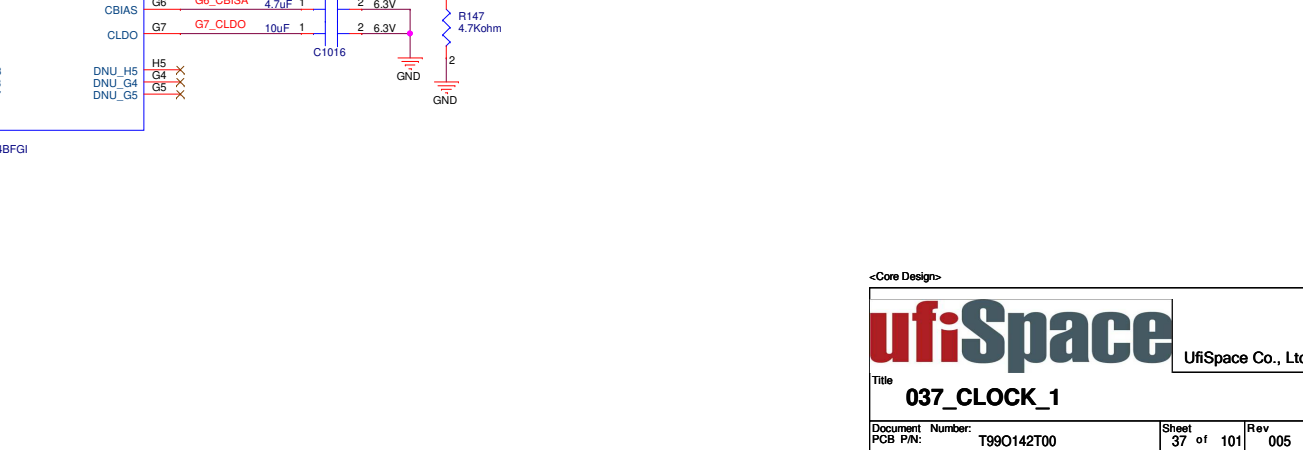
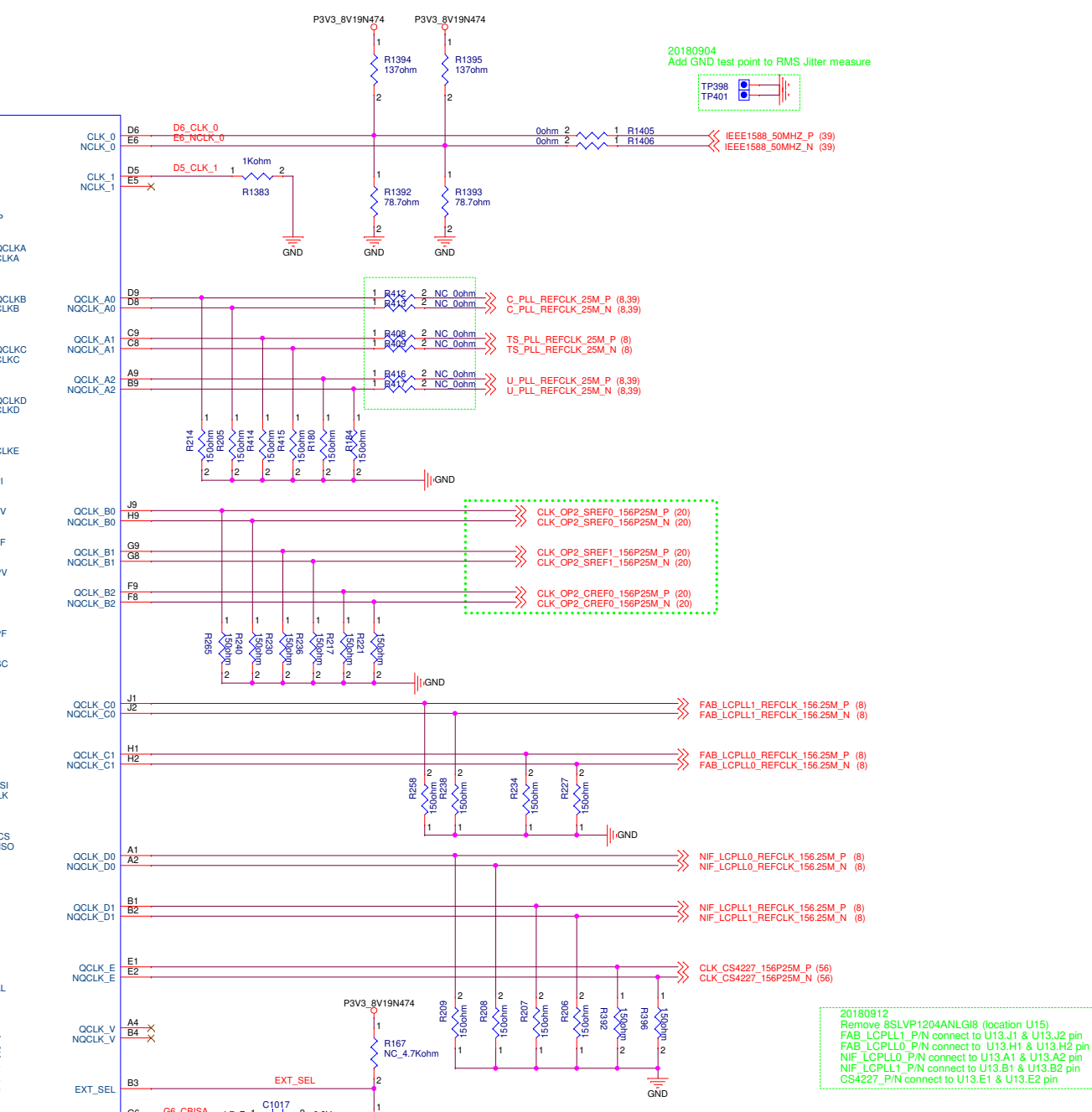
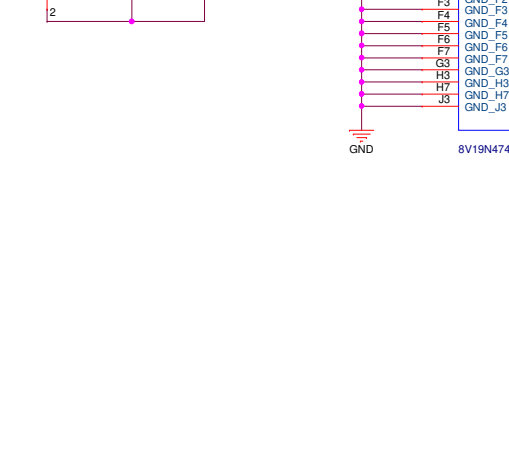
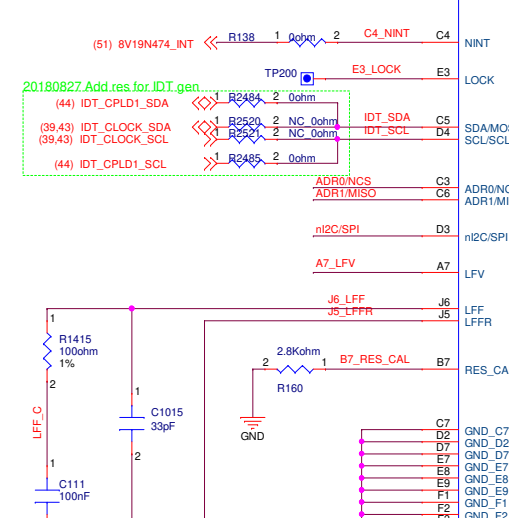
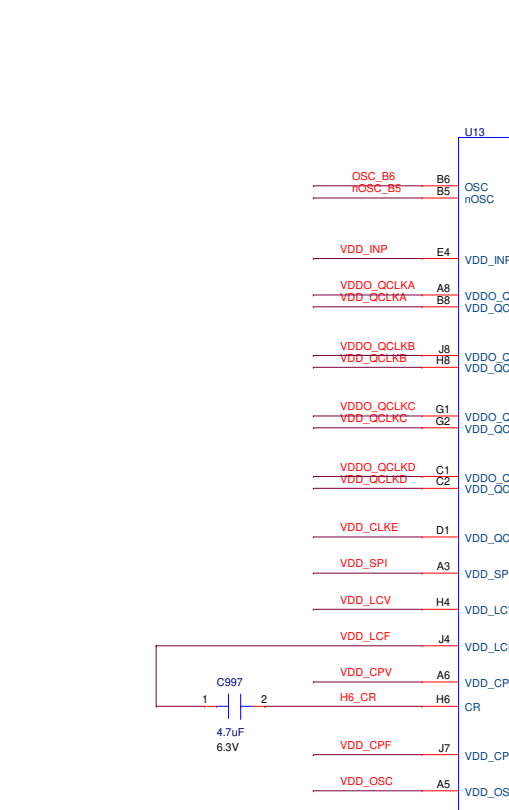
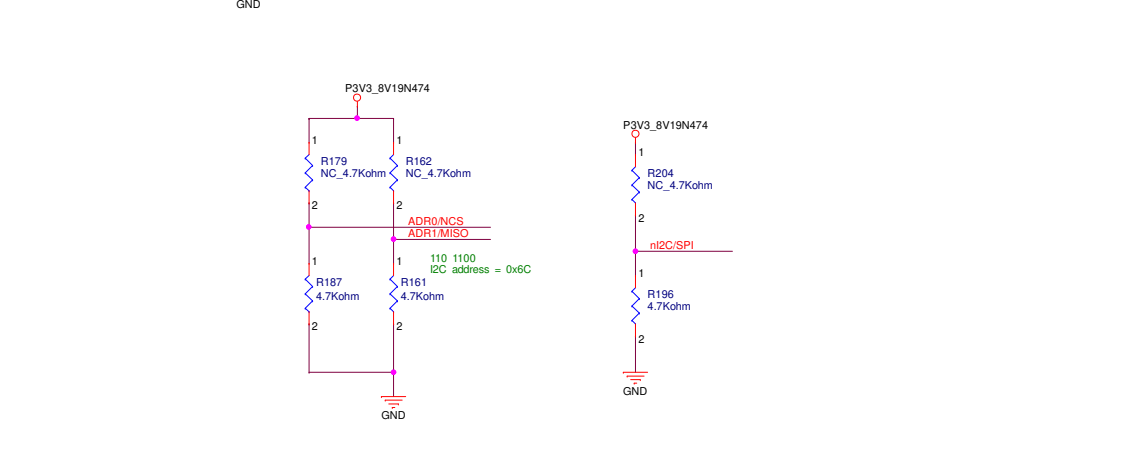
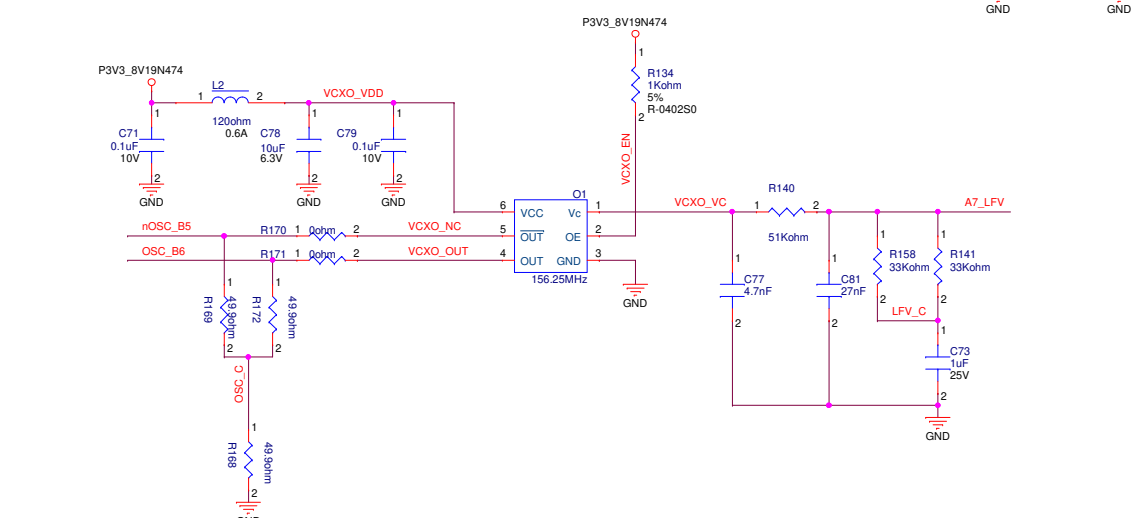
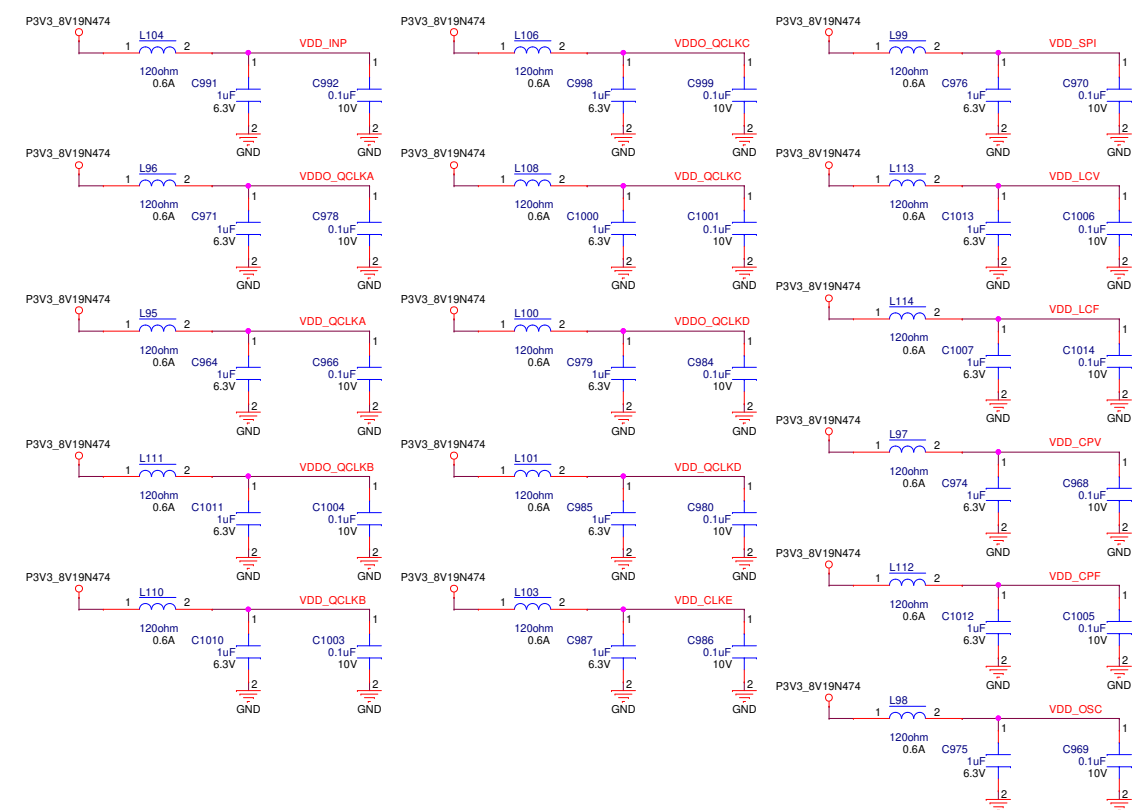


Blackhawk supports SerDes polarity inversion.

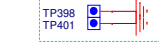
Figure 5 shows the basic structure of the fabric interface, including the fabric MAC (FMAC) and the Blackhawk SerDes. On the Blackhawk SerDes, no RX or TX mapping (swapping) exists. On the FMAC, only TX mapping (swapping) exists.



<Core Design>

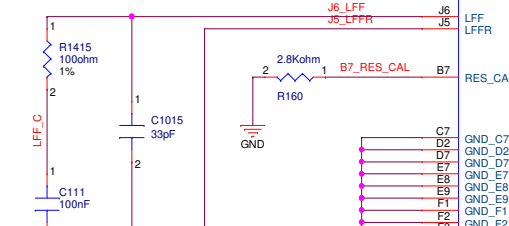


20180904
Add GND test point to RMS Jitter measure

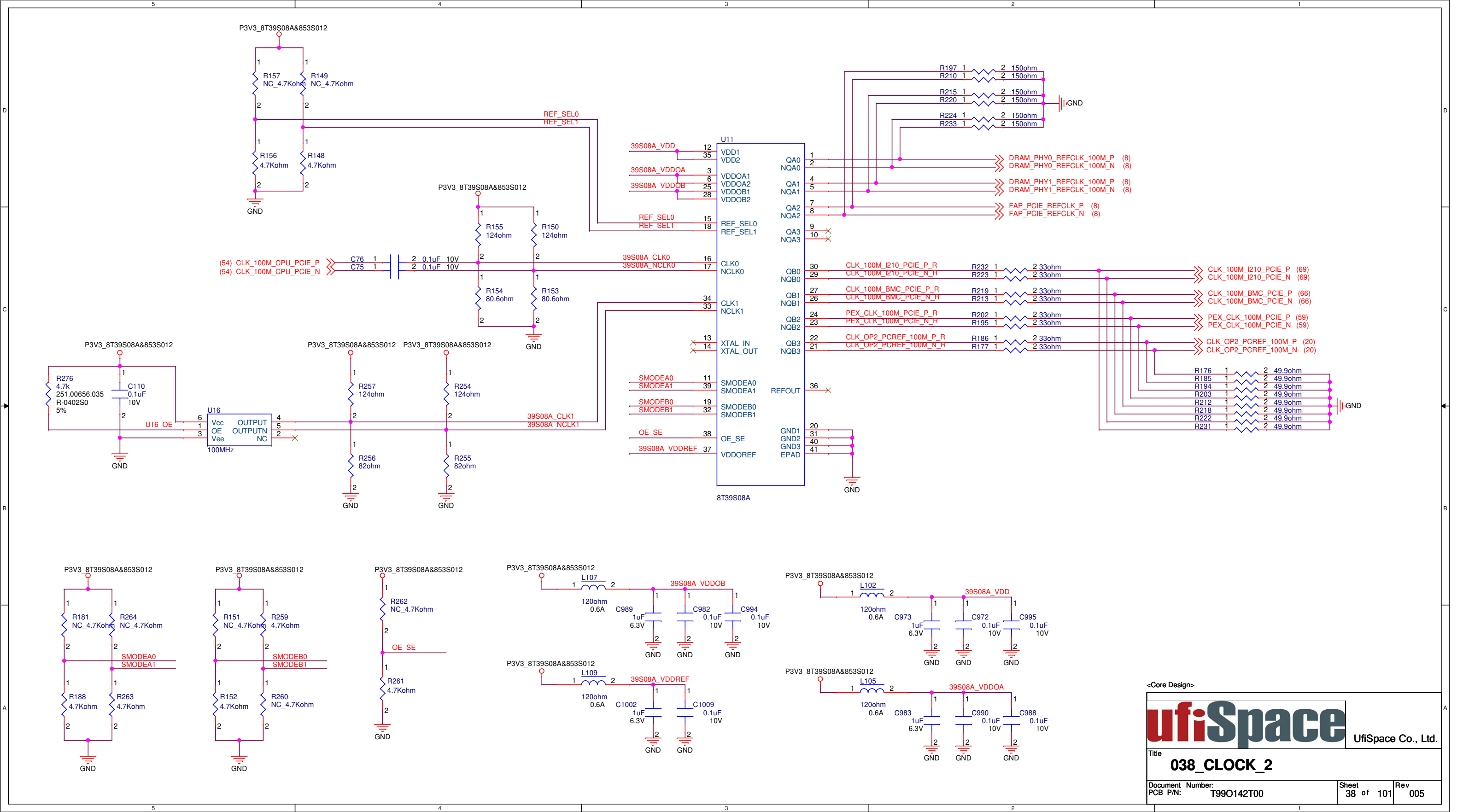


20180827.Add.res.for.IDT.gen...
(44) IDT_CPLD1_SDA << B2484 2 0ohm
(39,43) IDT_CLOCK_SDA << B2484 2 NC 0ohm
(39,43) IDT_CLOCK_SCL << B2484 2 NC 0ohm
(44) IDT_CPLD1_SCL << B2485 2 0ohm

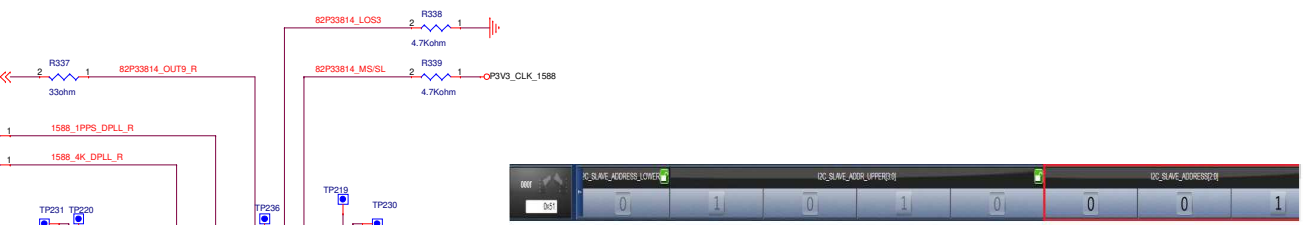
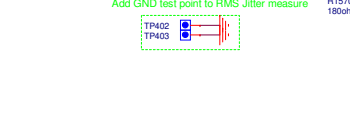
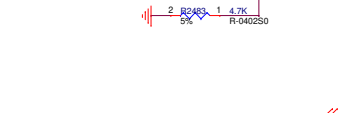
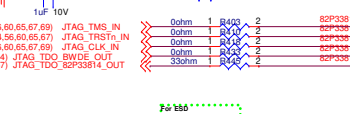
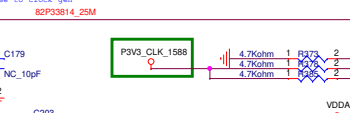
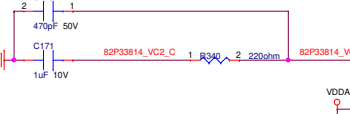
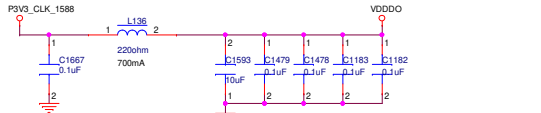
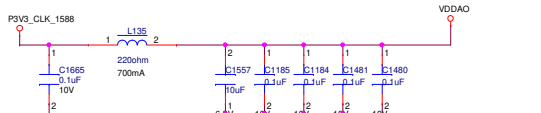
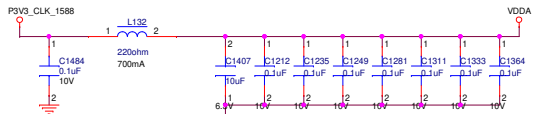
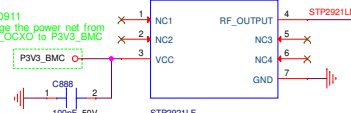
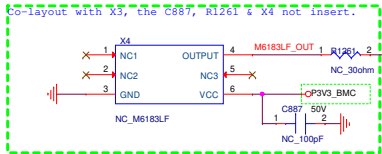
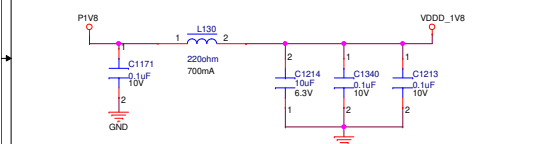
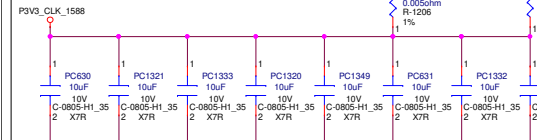
For IDT Clock Gen to upgrade code



20180912
Remove 8SLVP1204ANLG18 (location U15)
FAB_LCPLL1_P/N connect to U13.J1 & U13.J2 pin
FAB_LCPLL0_P/N connect to U13.H1 & U13.H2 pin
NIF_LCPLL0_P/N connect to U13.A1 & U13.A2 pin
NIF_LCPLL1_P/N connect to U13.B1 & U13.B2 pin
CS4227_P/N connect to U13.E1 & U13.E2 pin

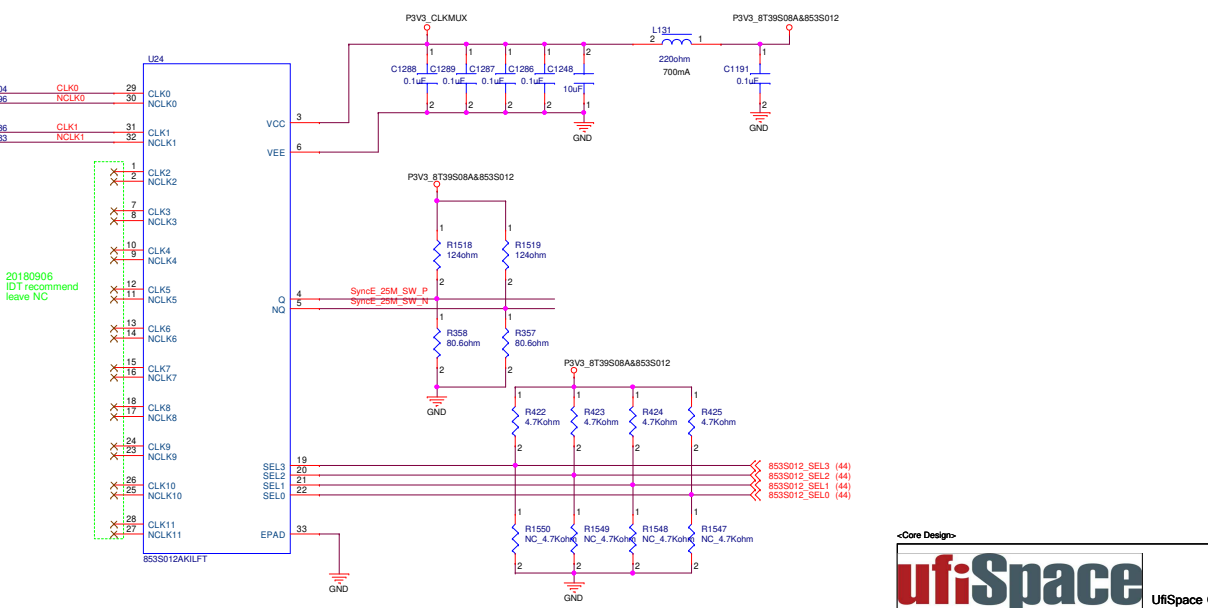
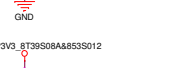
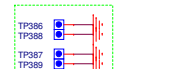
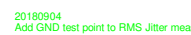
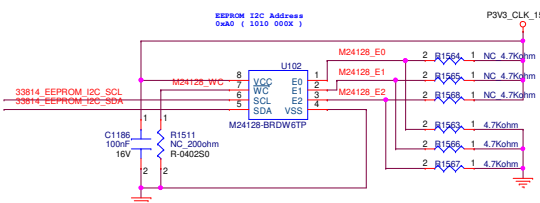
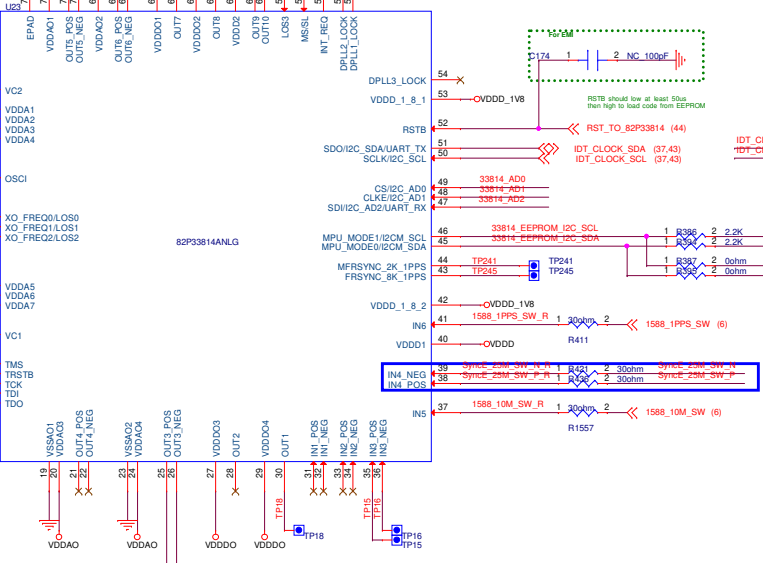
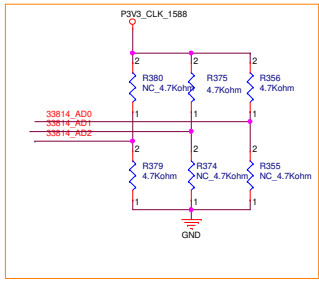


20180911
Remove PU1



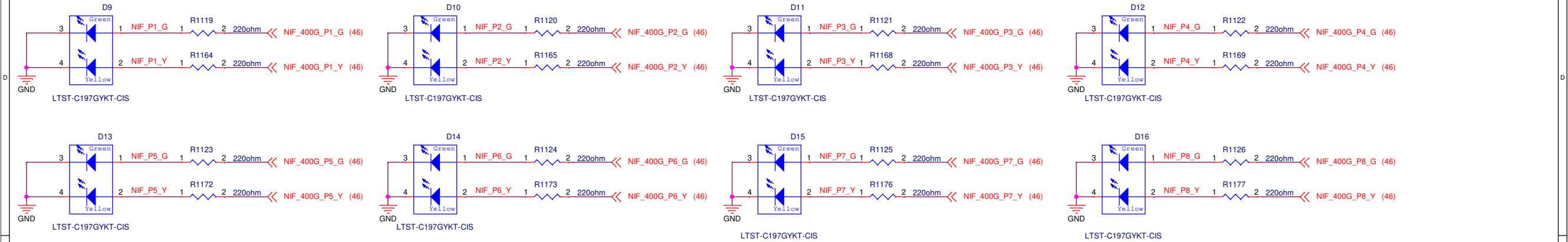
82P33814 default address
0x53 (0101 0011)

IDT comment:
There are I2C_AD[2:1] pins are the address bus for selecting device address. I2C_AD0 being ignored

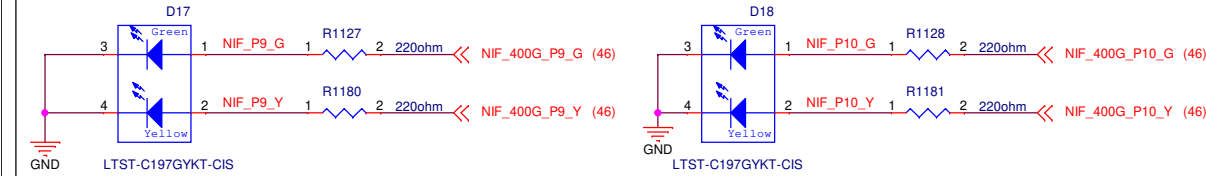


QSFPDD for NIF

Port 1 ~ Port 8



Port 9 ~ Port 10



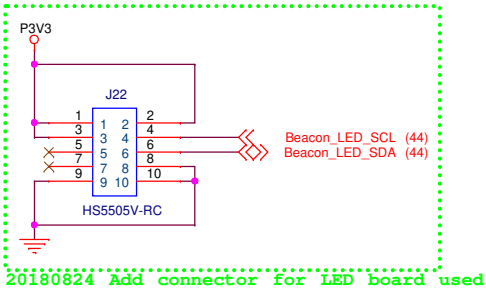
QSFPDD For FAB

Port 1 ~ Port 8

LED is actived-LOW



To LED BOARD CONNECTOR



<Core Design>

ufiSpace UfiSpace Co., Ltd.

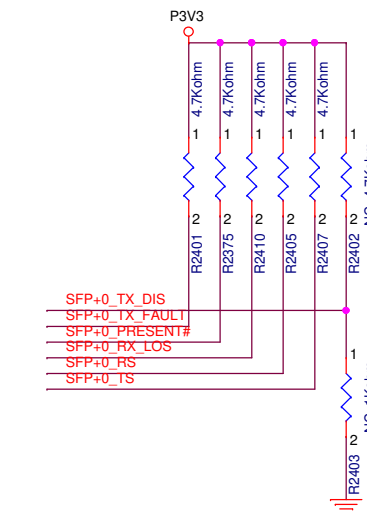
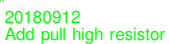
Title
040_LED CIRCUIT

Document Number:
PCB P/N: T99O142T00

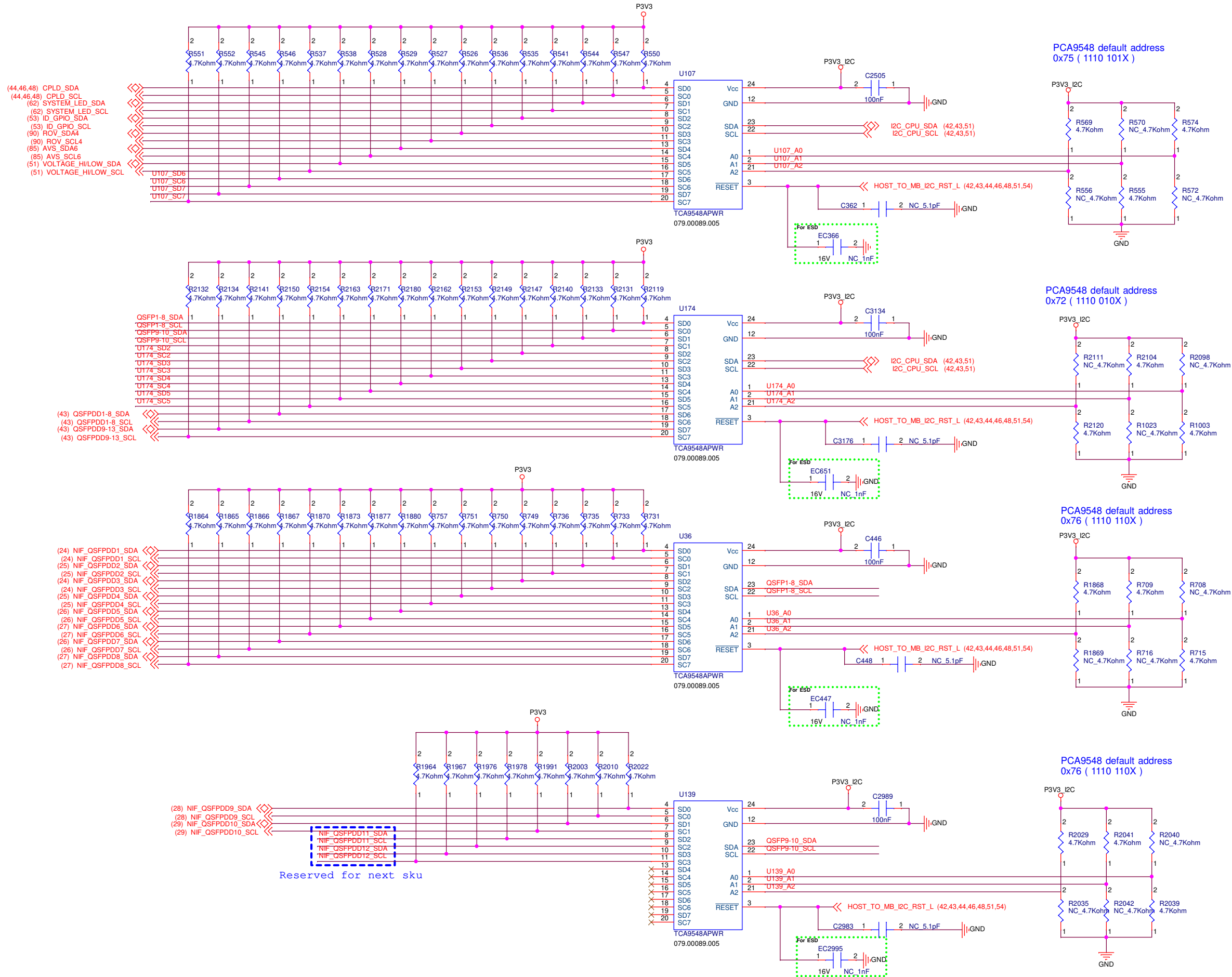
Sheet
40 of 101

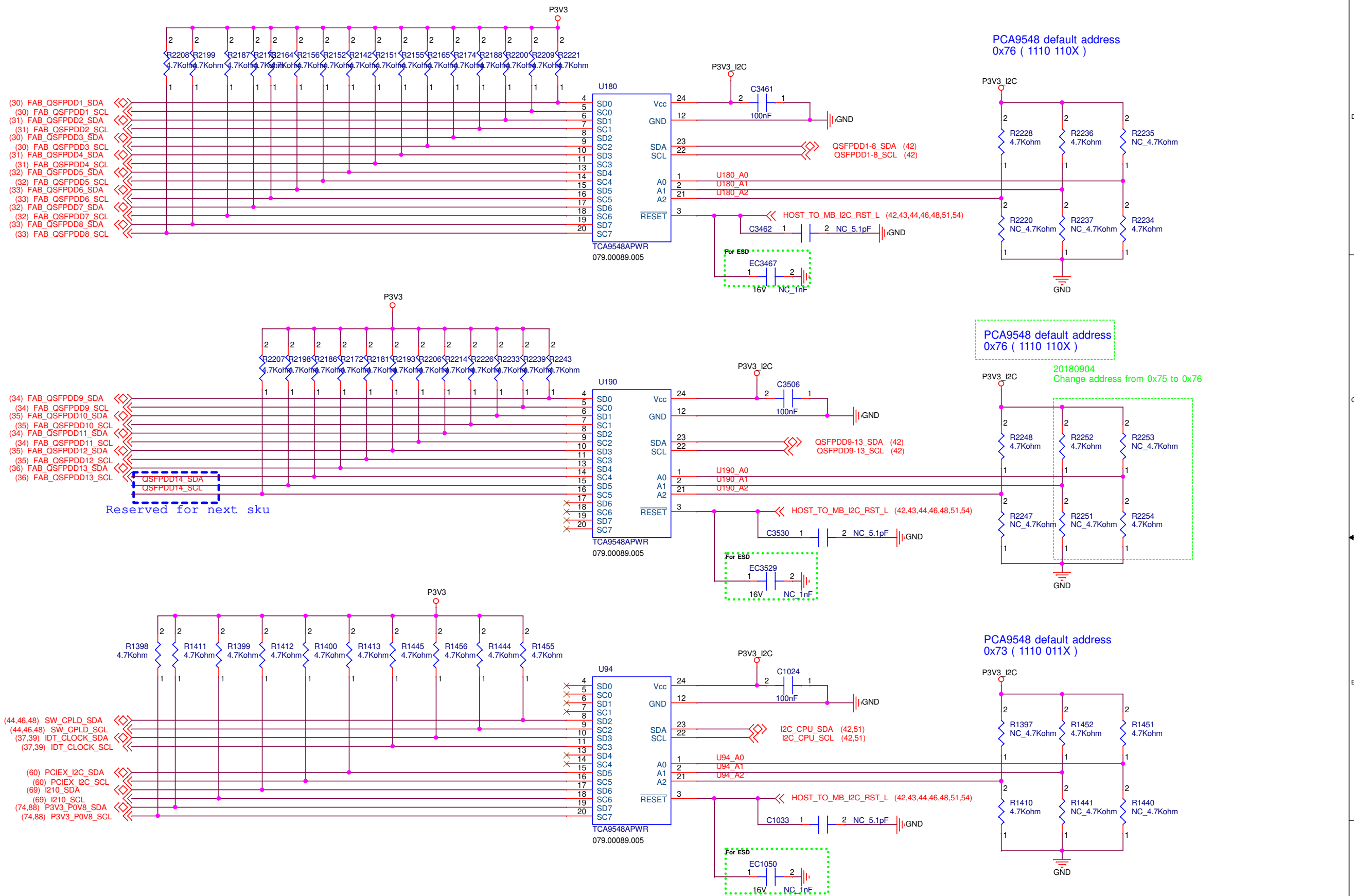
Rev
005

SFP[0:1]_TS (Rate Select)
- loutput of SFP
>1: Rate greater than 4.25Gb (default by HW)



Changed all IO expander power source from P3V3 to P3V3_I2C.



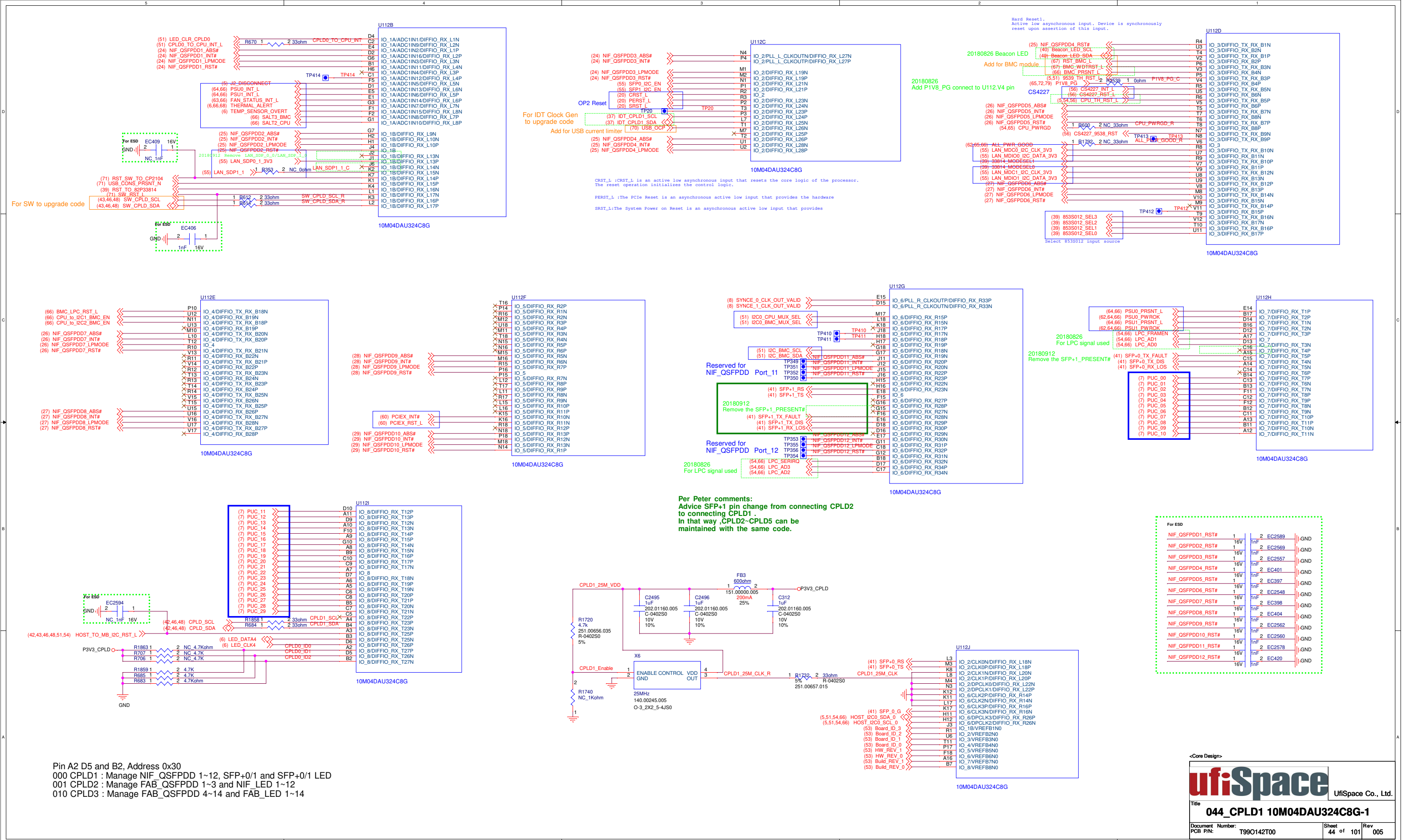


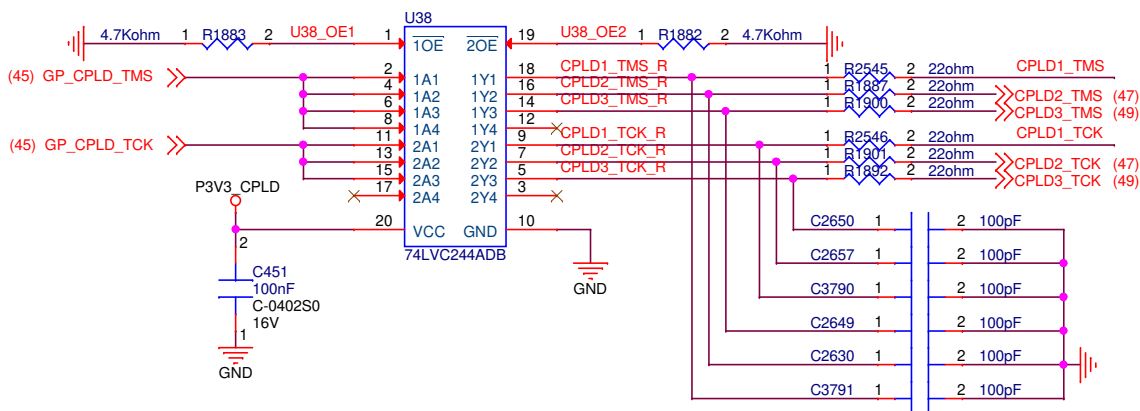
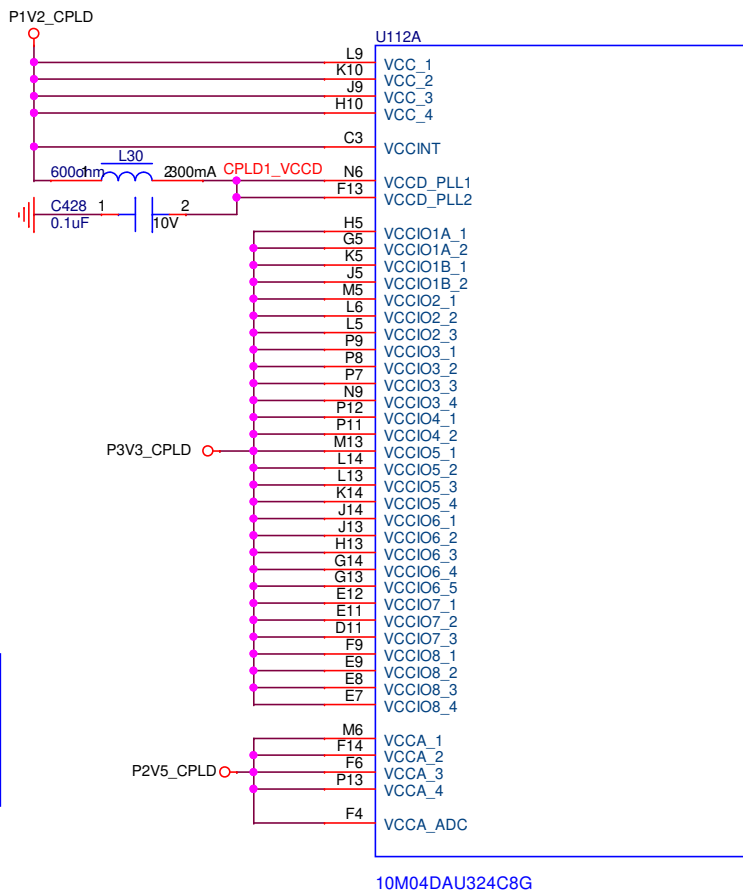
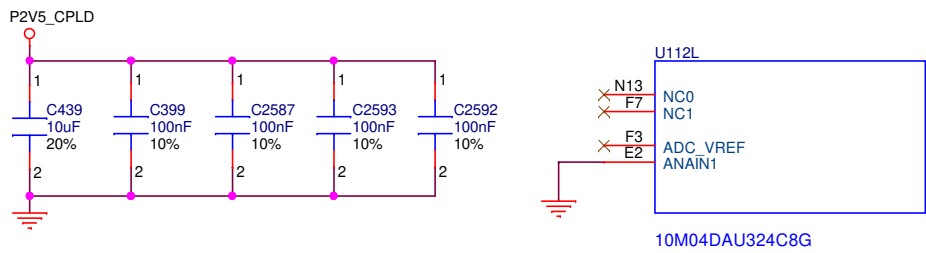
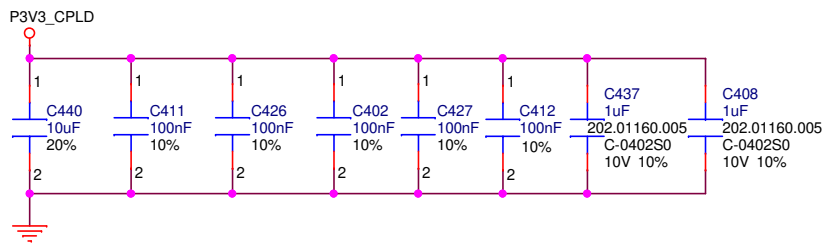
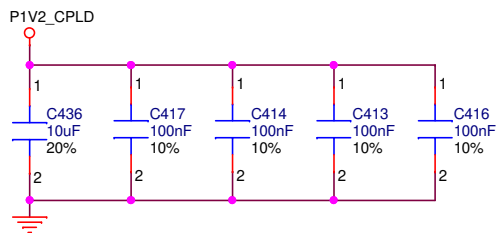
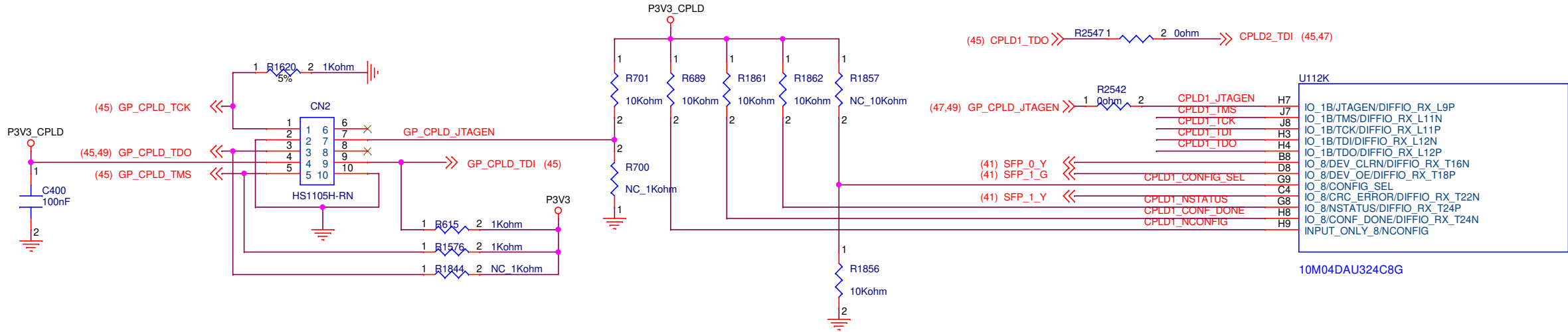
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0x76 (1110 110X)

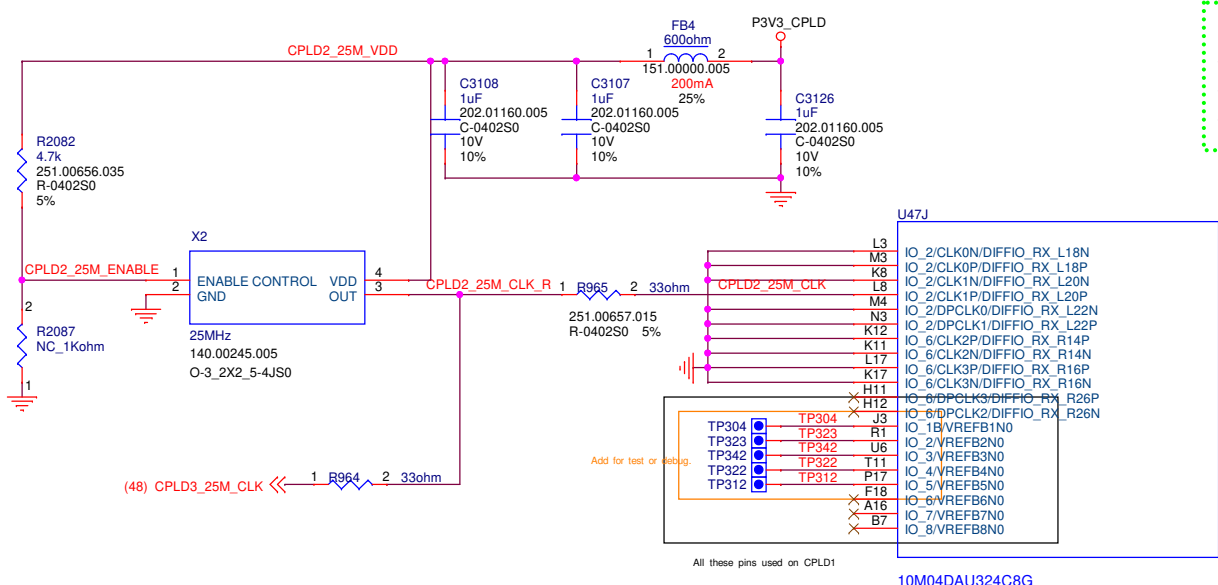
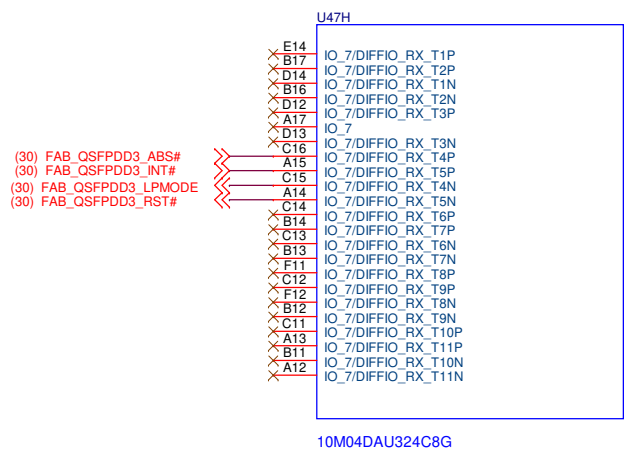
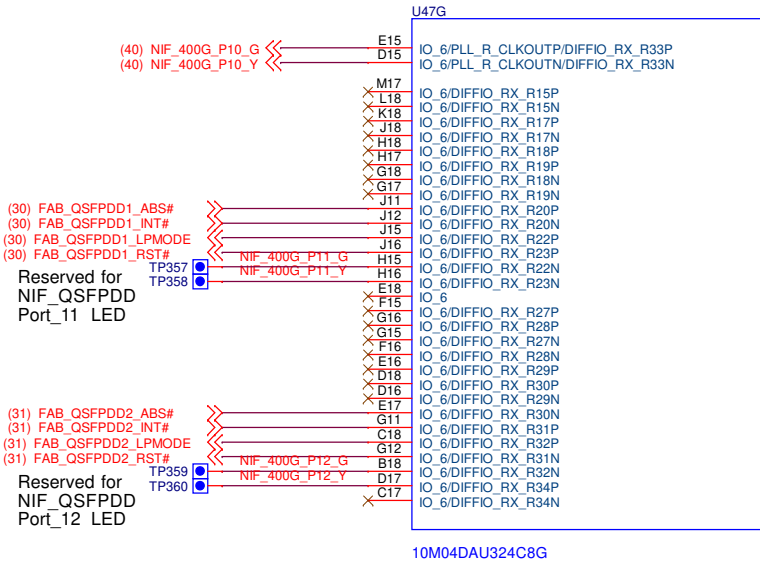
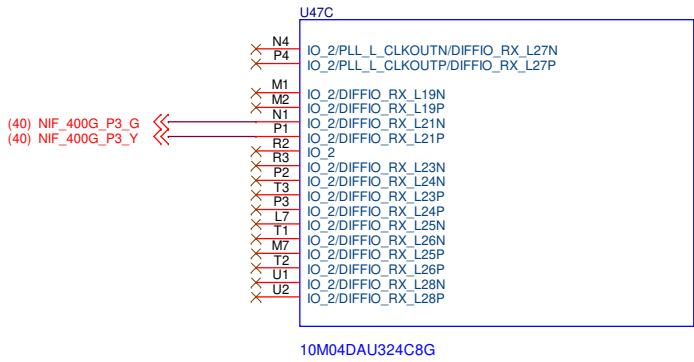
PCA9548 default address
0x76 (1110 110X)

20180904
Change address from 0x75 to 0x76

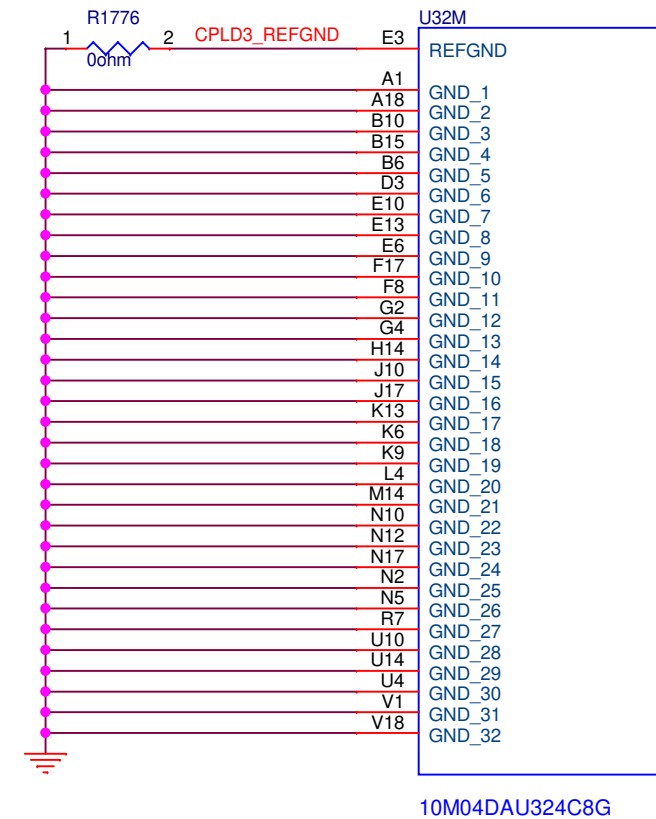
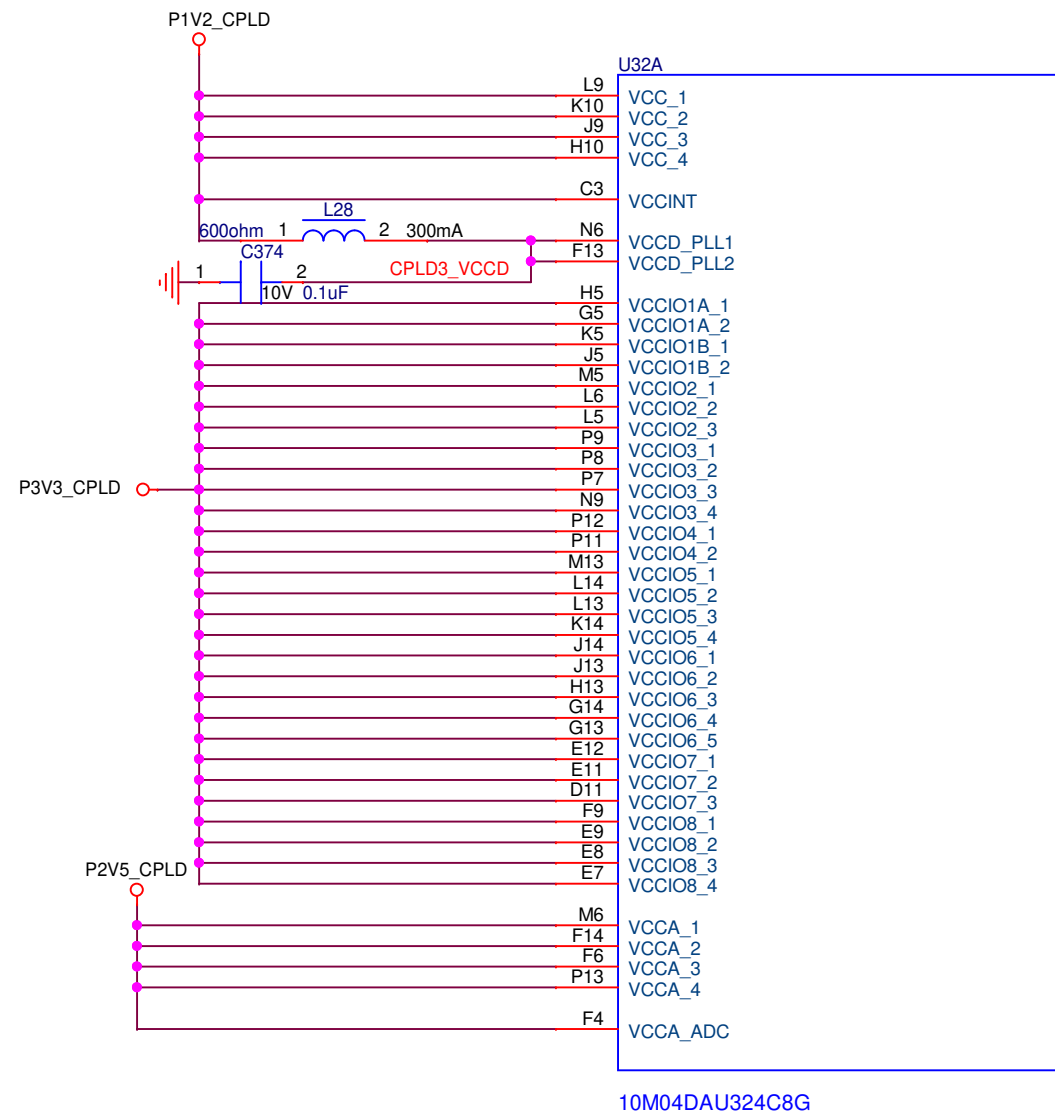
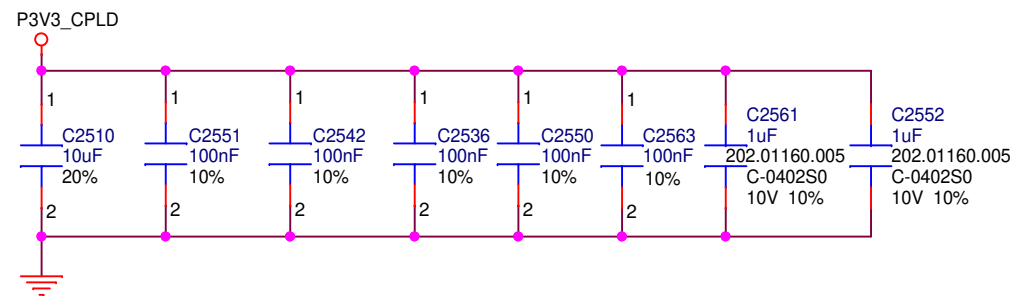
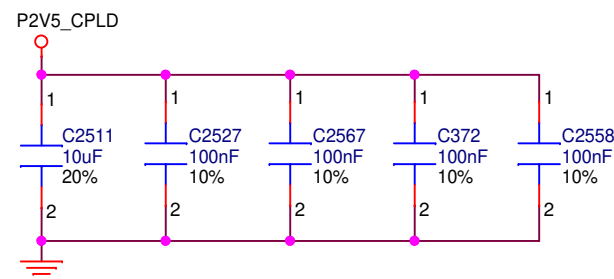
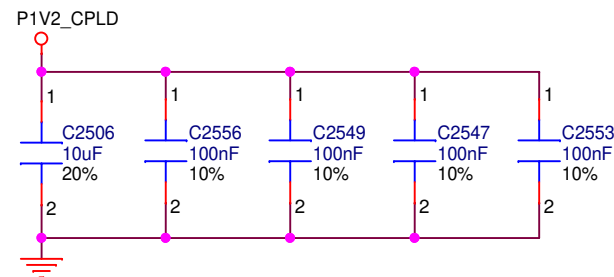
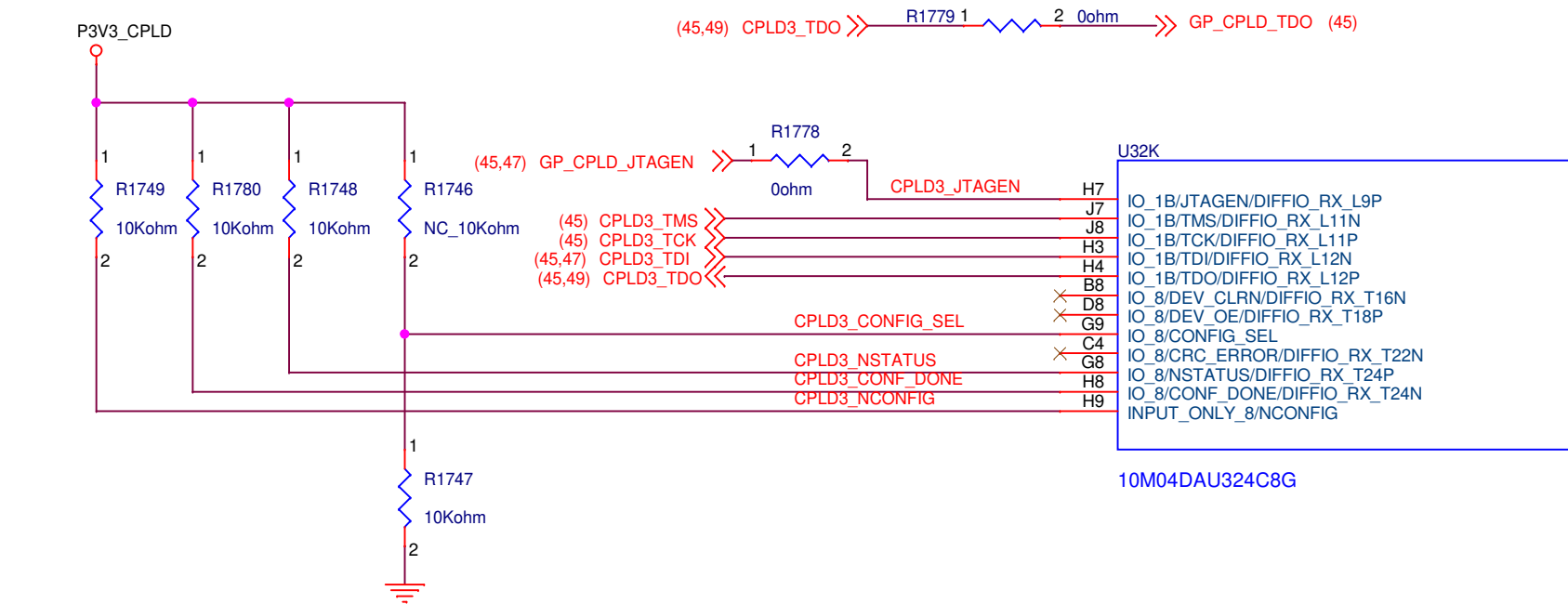
PCA9548 default address
0x73 (1110 011X)







The image shows the UfiSpace logo, which consists of the word "ufi" in red lowercase letters and "Space" in blue uppercase letters. To the right of the logo is the text "UfiSpace Co., Ltd." in black. Below the logo is a white rectangular box containing the product code "046_CPLD2 10M04DAU324C8G-1" in bold black text. At the bottom of the image is a white rectangular box containing the text "Document Number: T990142T00" on the left and "Sheet 46 of 101" on the right, with "Rev 005" on the far right.

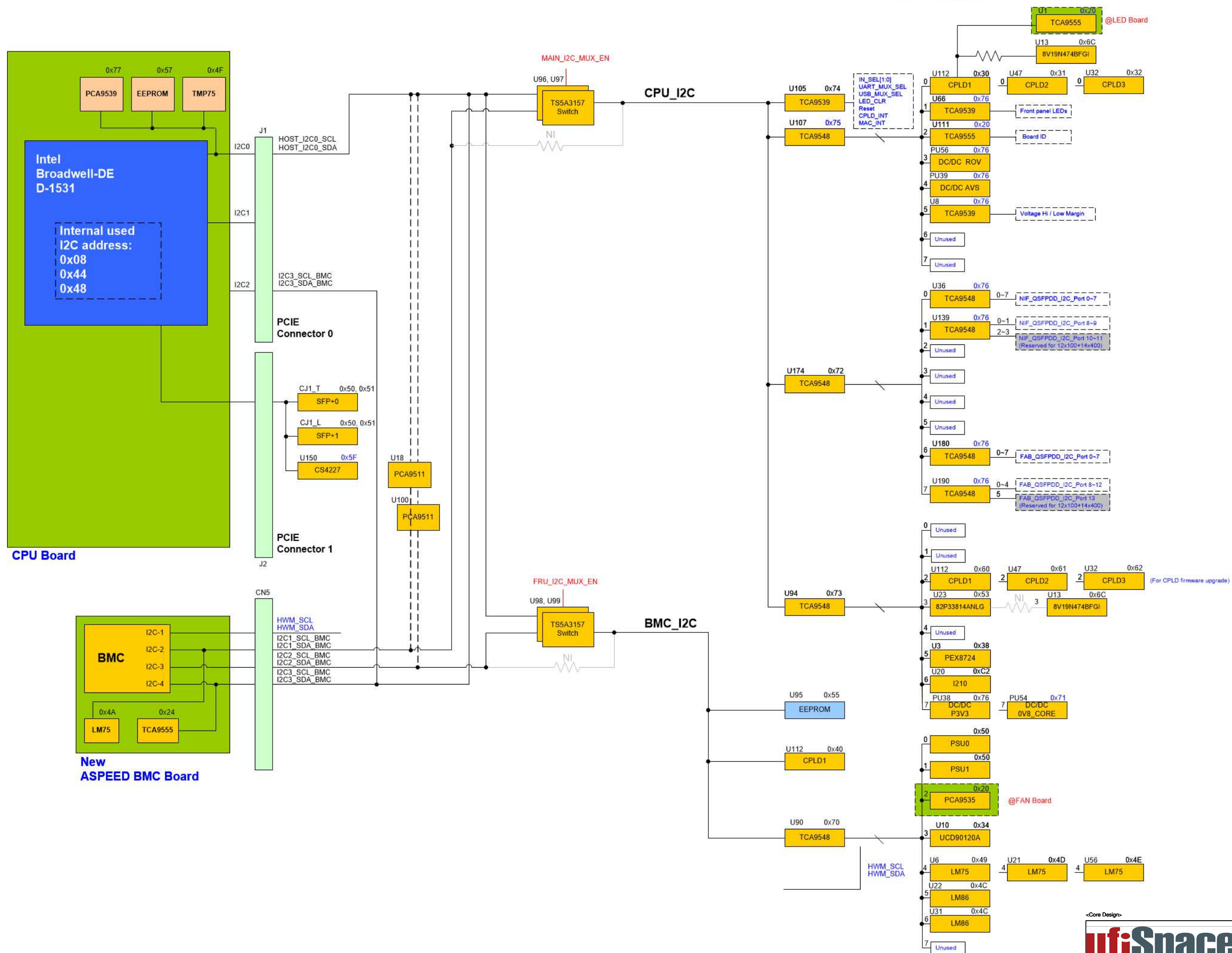


<Core Design>

ufiSpace UfiSpace Co., Ltd.

Title: **049_CPLD3 10M04DAU324C8G-2**

Document Number: T99O142T00 Sheet 49 of 101 Rev 005



CPU_I2C

BMC_I2C

Changed all power source from P3V3 to P3V3_I2C.

EEPROM
0x55 (7b' 0101)

Add AND gate for CPLD0 and CPLD1 interrupt.

<Core Design>

ufiSpace

UfiSpace Co., Ltd.

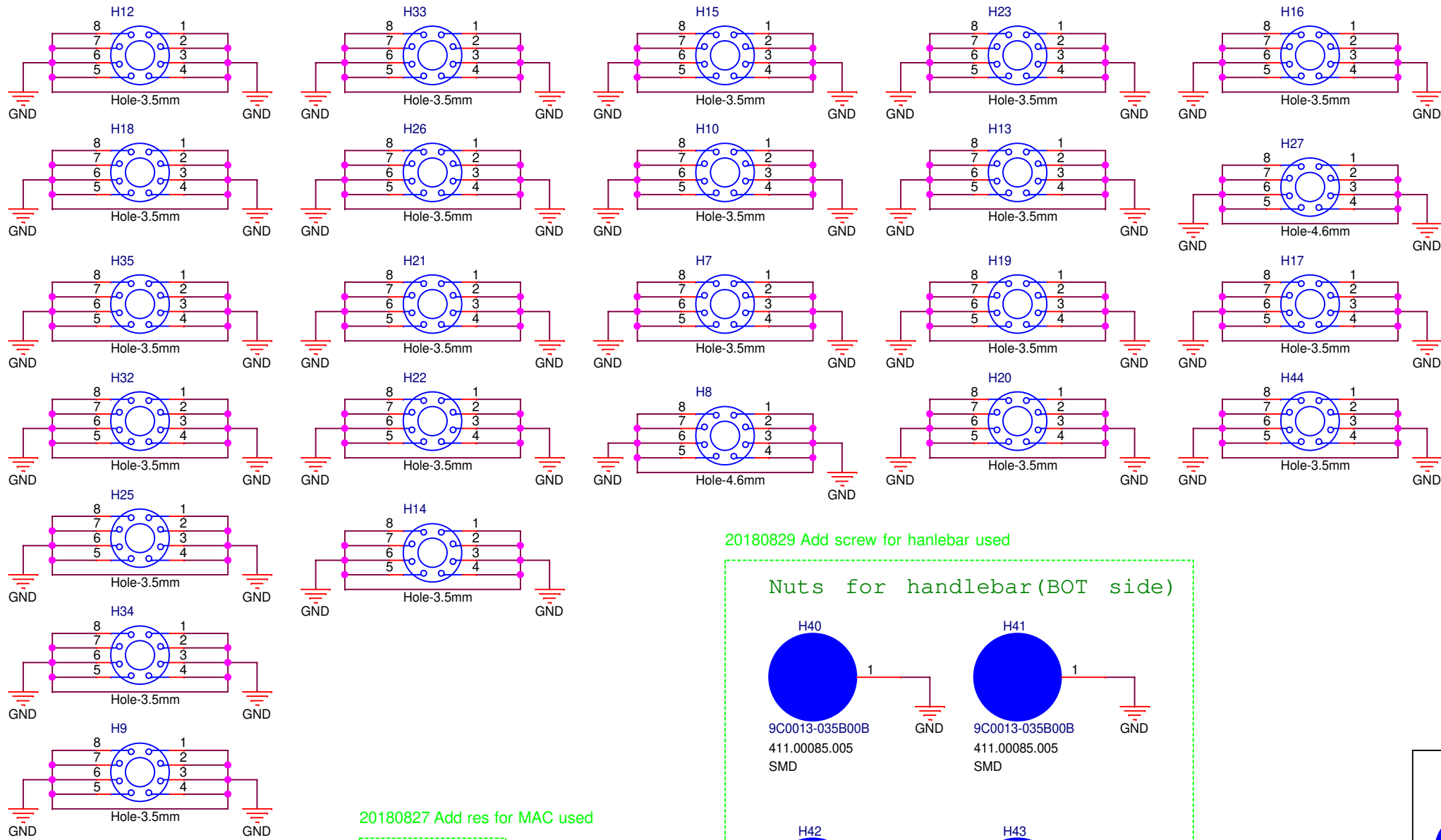
Title
051_I2C_SYSTEM

Document Number:
PCB P/N: T990142T00

Sheet
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Rev
005

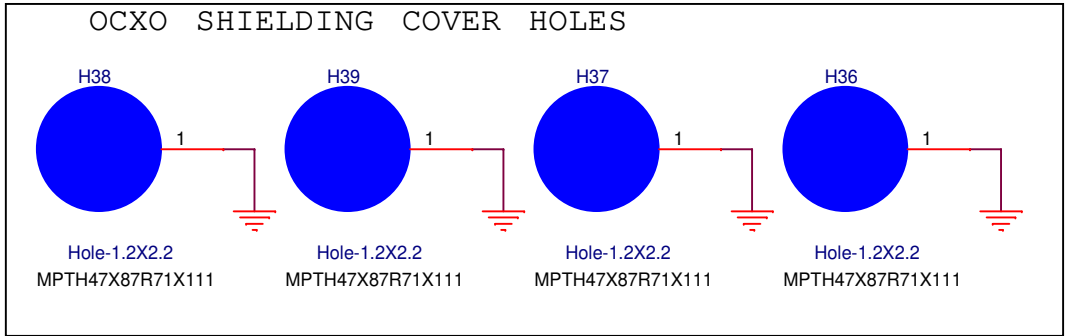
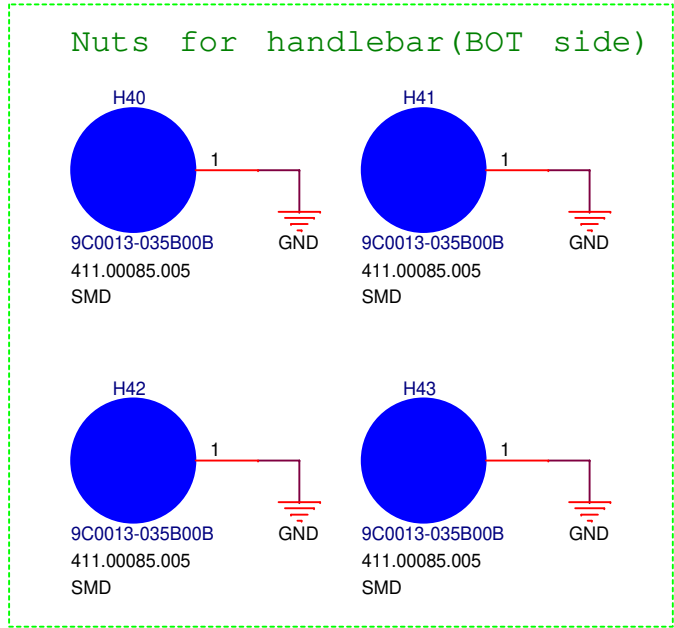
MOUNTING HOLE Mounting Hole = 3.5mm



20180827 Add res for MAC used

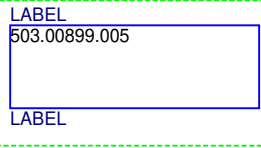


20180829 Add screw for hanlebar used



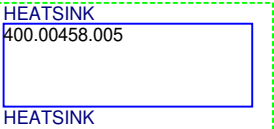
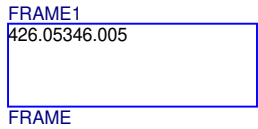
BOM ONLY PARTS

20180910
Change LABEL part number
from 503.01032.005 to 503.00899.005

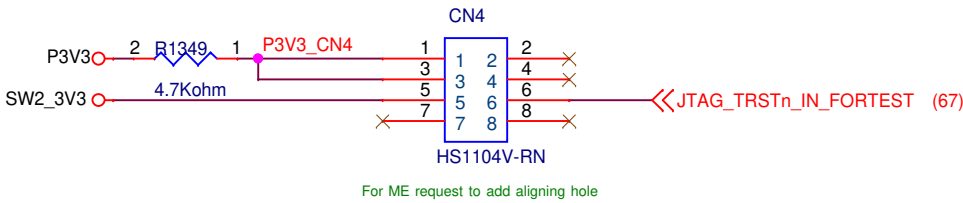


20180910
Remove LABEL1,
LABEL2 & LABEL3

20180905 Remove Battery



20180905
Add Heatsink for PCIE switch



<Core Design>

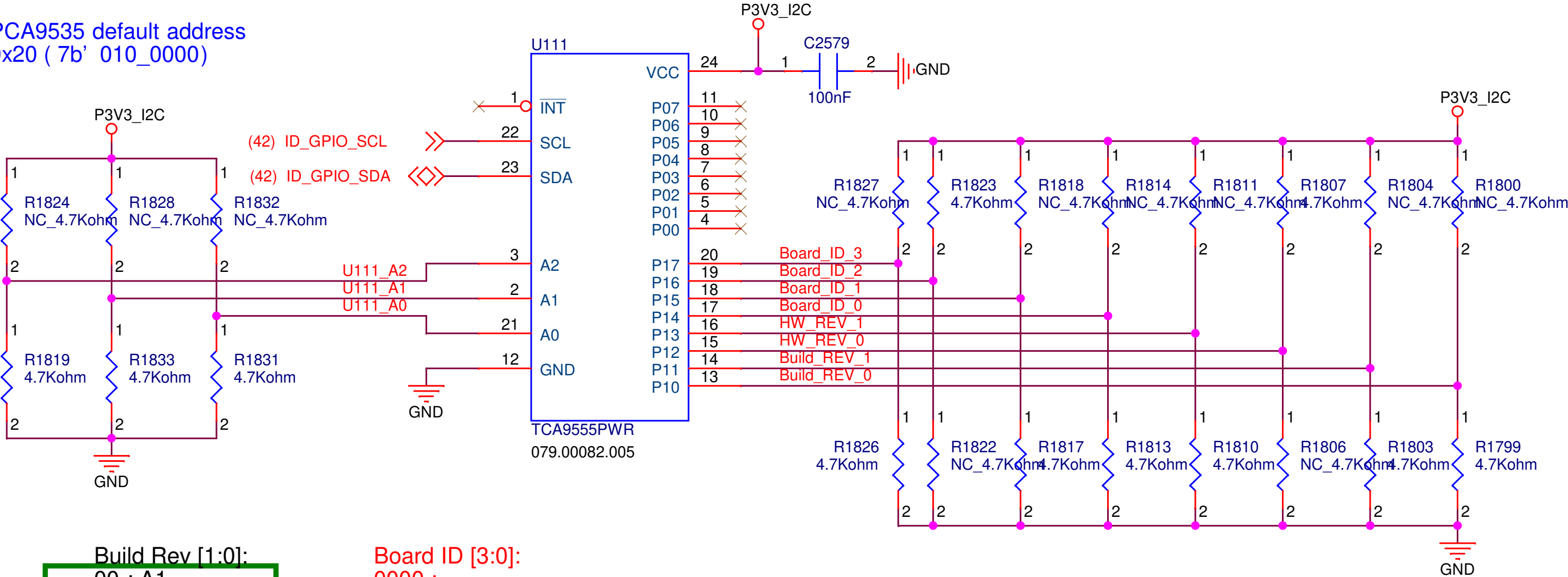


UfiSpace Co., Ltd.

Title 052_SCREW		
Document Number: PCB P/N:	T990142T00	Sheet 52 of 101 Rev 005

Changed all power source from P3V3 to P3V3_I2C.

PCA9535 default address
0x20 (7b' 010_0000)



Build Rev [1:0]:

00 : A1
01 : A2
10 : A3
11 : A4

Hardware Revision [1:0]:

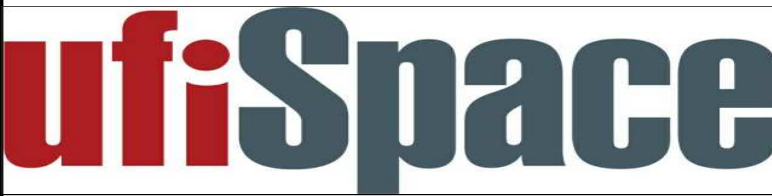
Proto : 00
Alpha : 01
Beta : 10
PVT : 11

Board ID [3:0]:

0000 :
0001 : APACHE SIAD
0010 : NCP1-1
0011 : NCP1-2
0100 : NCP2-1
0101 : NCP2-2
0110 :
0111 :
1000 :
1001 :
1010~1111: Reserved

Board_ID_3 >> Board_ID_3 (44)
Board_ID_2 >> Board_ID_2 (44)
Board_ID_1 >> Board_ID_1 (44)
Board_ID_0 >> Board_ID_0 (44)
HW_REV_1 >> HW_REV_1 (44)
HW_REV_0 >> HW_REV_0 (44)
Build_REV_1 >> Build_REV_1 (44)
Build_REV_0 >> Build_REV_0 (44)

<Core Design>

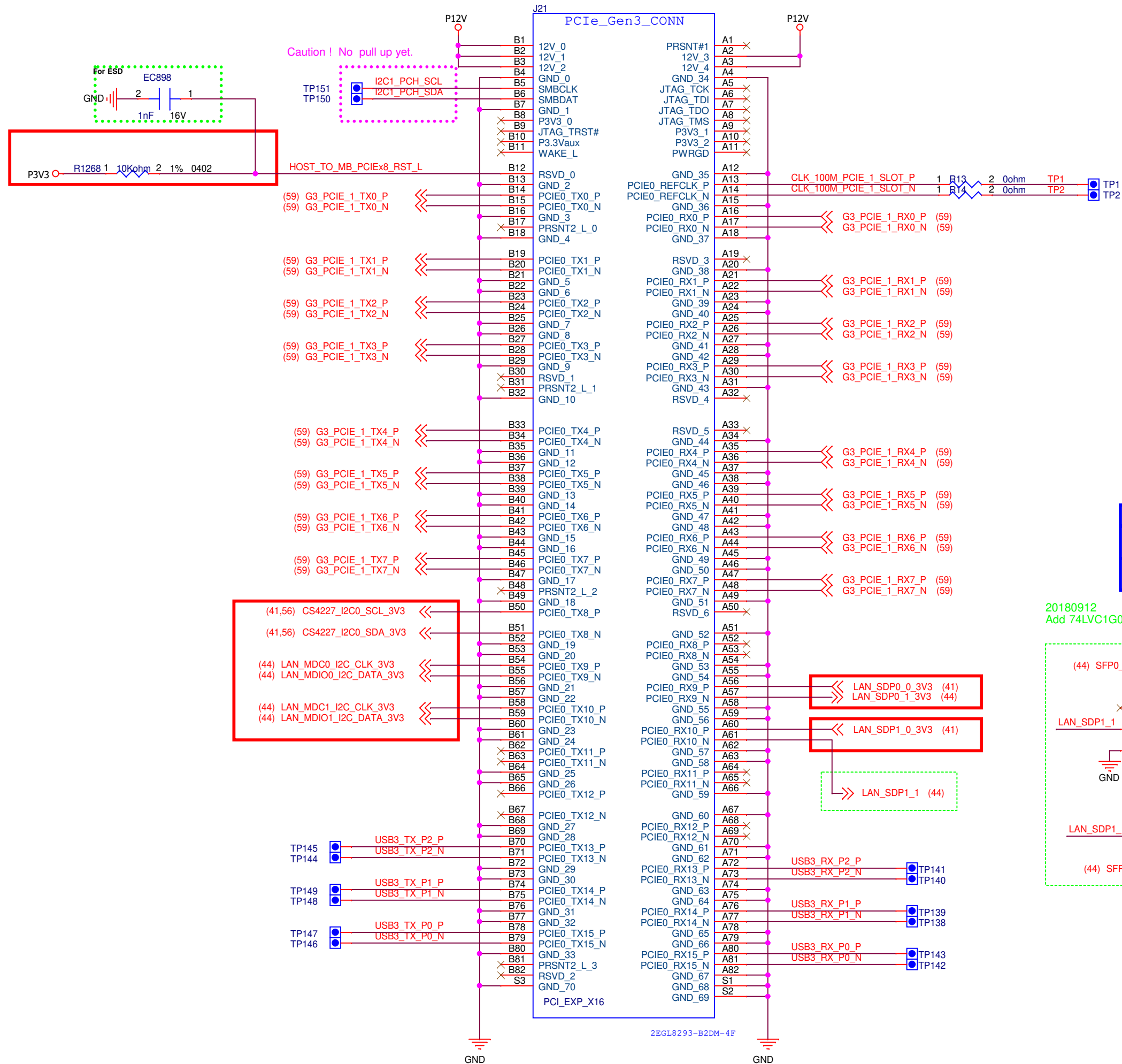


UfiSpace Co., Ltd.

Title
053_SWITCH INT

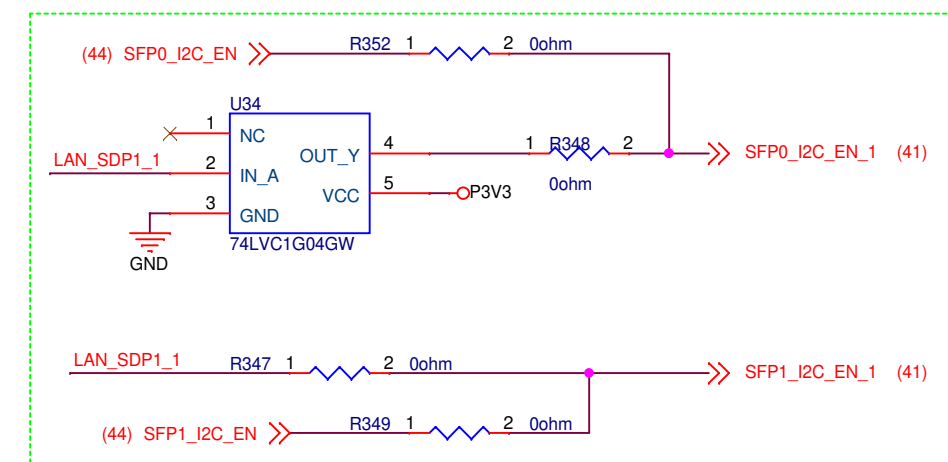
Document Number:
PCB P/N: T99O142T00

Sheet
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Rev
005



LAN_SDP1_1	SFP0_I2C_EN_1	SFP1_I2C_EN_1
0	1	0
1	0	1

20180912
Add 74LVC1G04 for SFP0/SFP1_I2C_EN used



<Core Design>

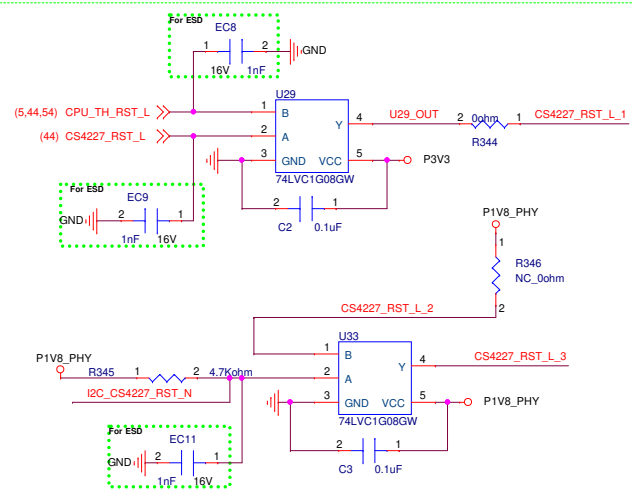
ufiSpace UfiSpace Co., Ltd.

Title
055_PCIE CONNECTOR_1

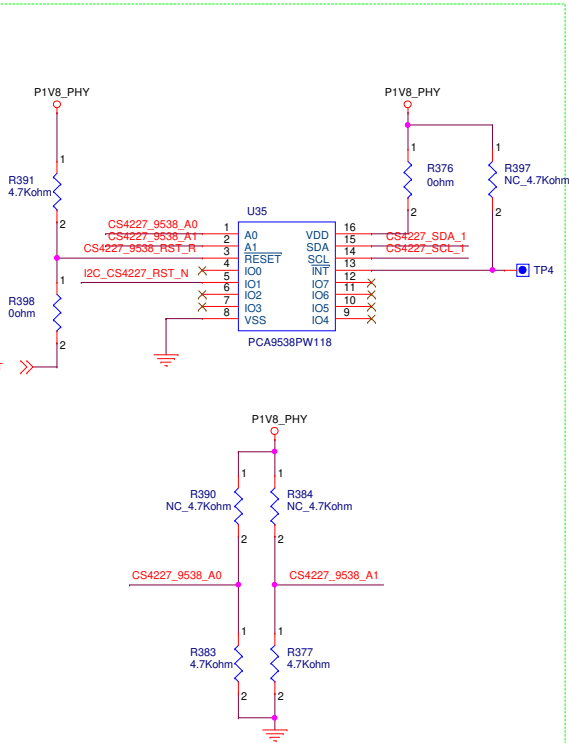
Document Number: T990142T00
PCB P/N: T990142T00

Sheet 55 of 101
Rev 005

20180912
Add AND Gate for CS4227 RST used

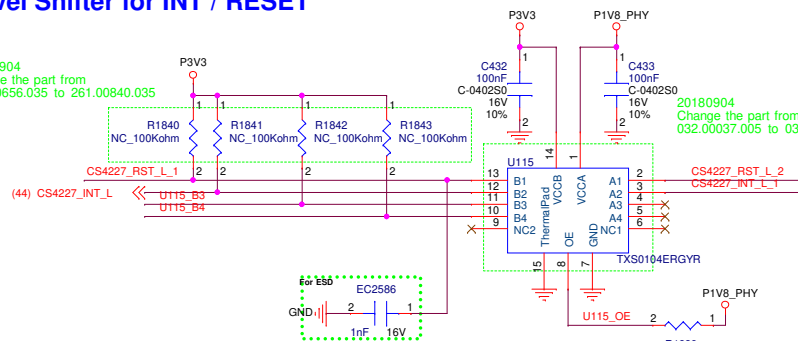


20180913
Add the I/O expander for CS4227 I2C

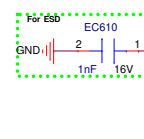


Level Shifter for INT / RESET

20180904
Change the part from
251.00656.035 to 261.00840.035

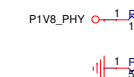


Tie to 1.8V for 1.2V I/O voltage levels
Float or tie to 0V for 1.8V/2.5V I/O voltage levels



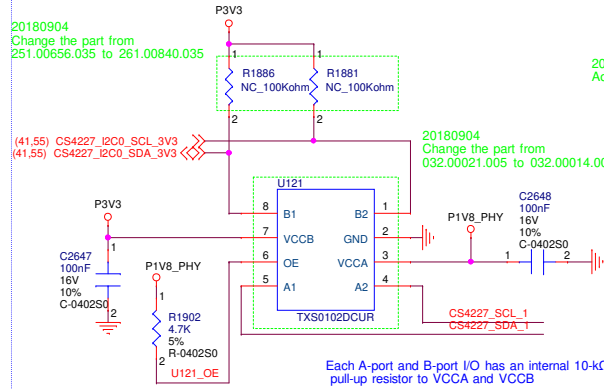
If REF_CLK exceeds 180 MHz, then tie REFDIV2_ENB low.
If REF_CLK is 180 MHz or less, tie REFDIV2_ENB high.

P1V8_PHY 1 R921 2 10Kohm REFDIV2_ENB
1% R0402S0

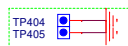


Level Shifter for MDC / MDIO

20180904
Change the part from
251.00656.035 to 261.00840.035



20180904
Add GND test point to RMS Jitter measure

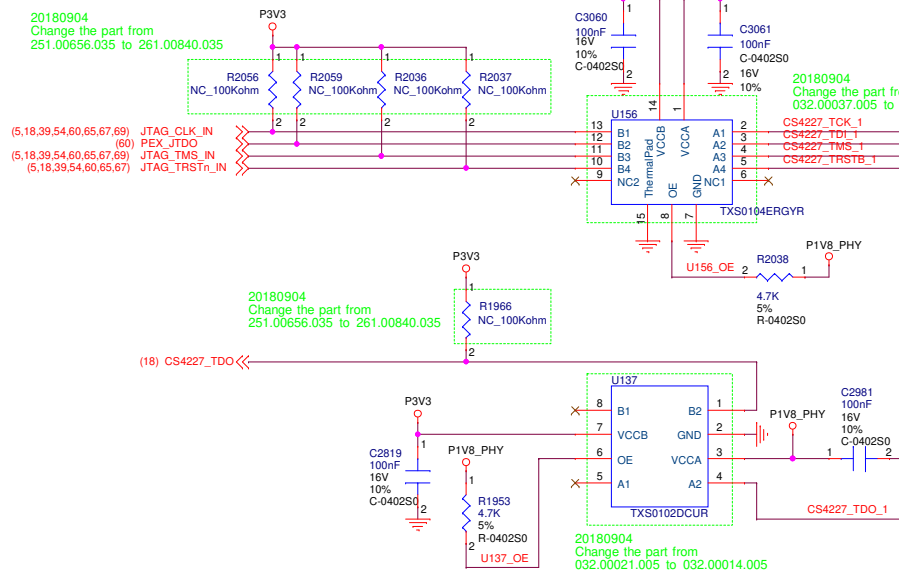


The CS4227 PHY reference clock inputs REF_CLK P/N may be connected directly to a differential source (without AC coupling capacitors) provided the specified Input Voltage Range (Table 45) is not exceeded for either the P or N inputs.

MICROSEL1	MICROSEL0	MODE
1	0	MDIO
0	1	I2C
0	0	I2C (Fast)

Level Shifter for JTAG Interface

20180904
Change the part from
251.00656.035 to 261.00840.035



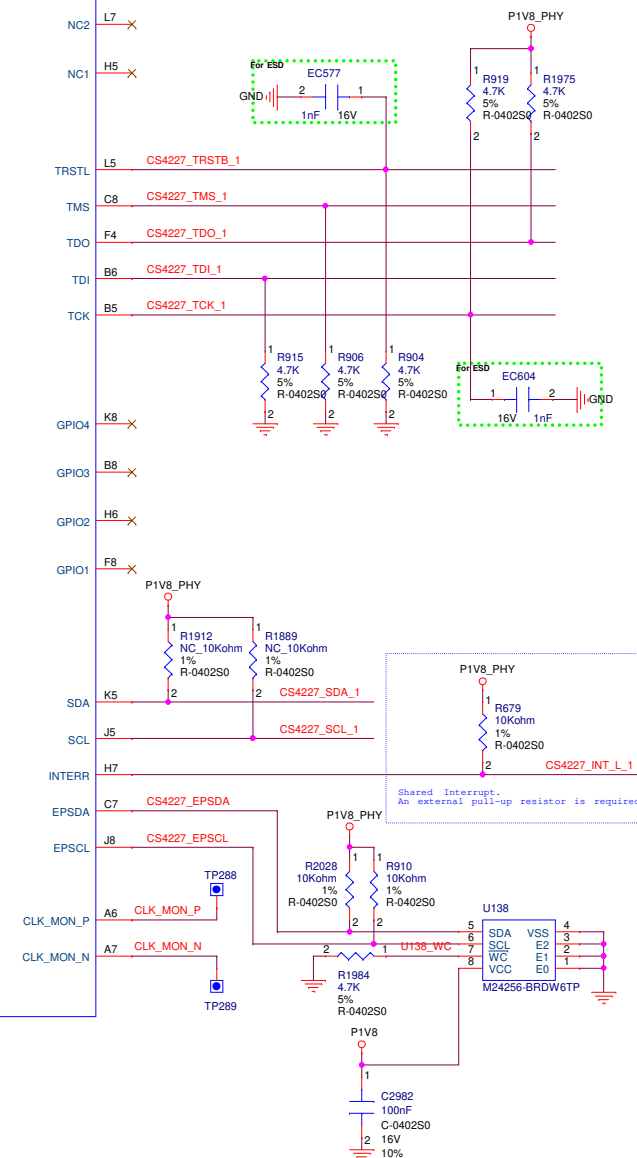
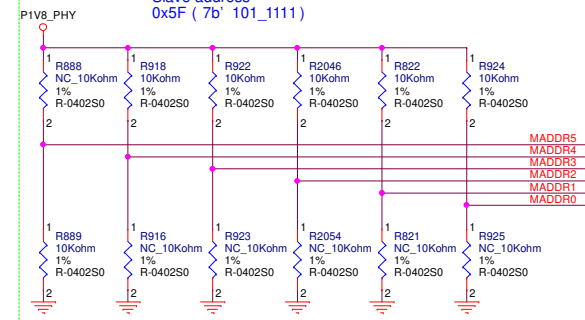
20180904
Change the part from
032.00037.005 to 032.00034.005

4.7
5%
R-

20180904
Change the part from
032.00021.005 to 032.00014.005

20180907 Change address to 0x5F

Slave address
0x5F (7b' 101_1111)



Shared Interrupt.
An external pull-up resistor is required.

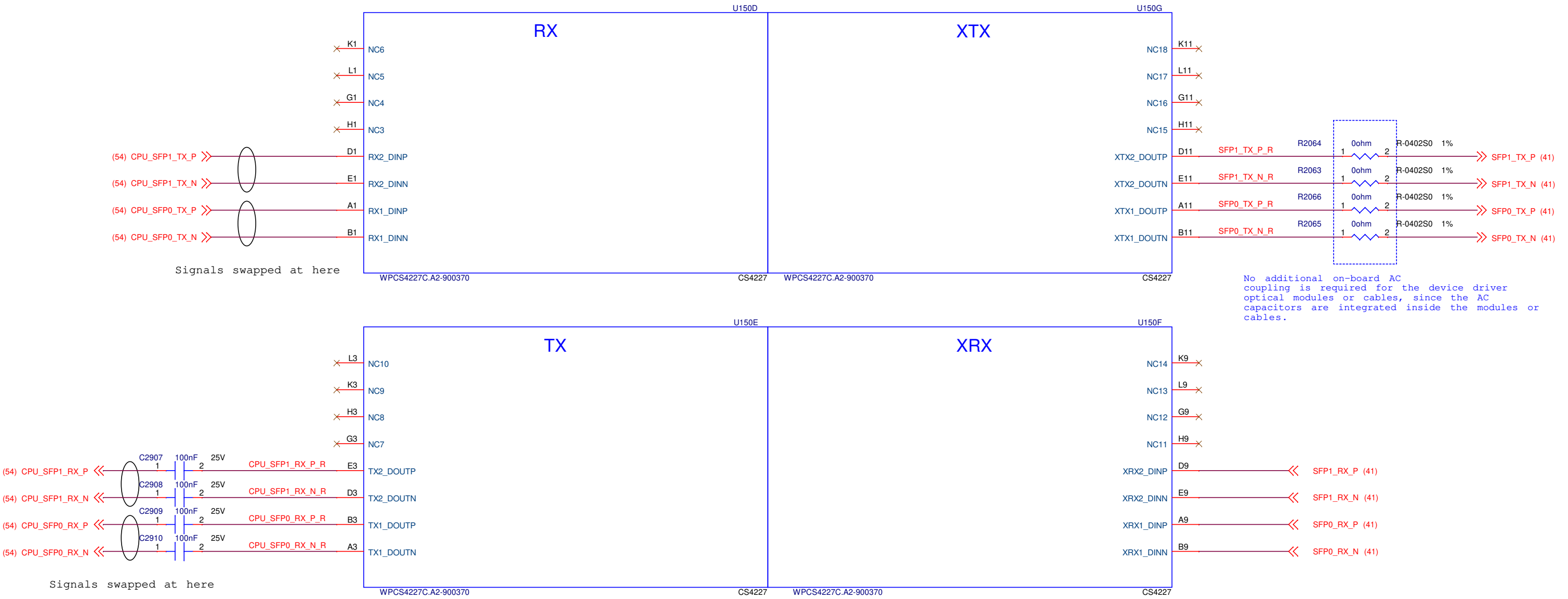
<Core Design>

ufiSpace UfiSpace Co., Ltd.

Title		056_CS4227_RESET_CLK_JTAG	
Document Number:	T990142T00	Sheet 56 of 101	Rev 005

Line Data (From CPU)

Host Data (To SFP+)

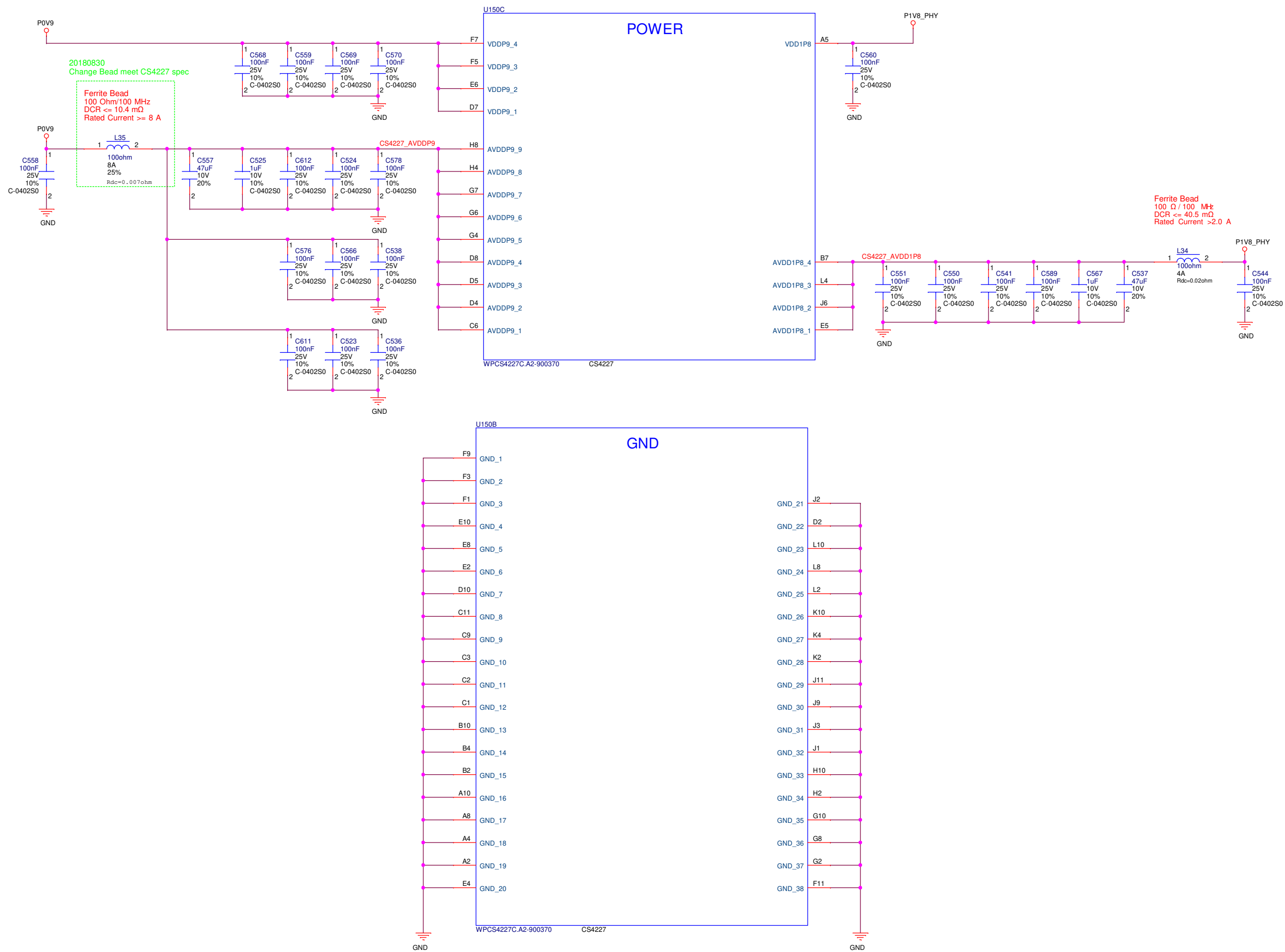


<Core Design>

ufiSpace UfiSpace Co., Ltd.

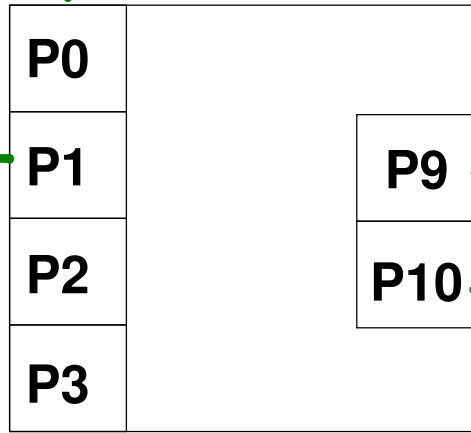
Title: **057_CS4227_PHY**

Document	Number:	Sheet	Rev
PCB P/N:	T99O142T00	57 of 101	005



Host CPU1
(Lane0~7)

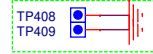
Host CPU0
(Lane8~11)



J2
(Lane24~27)

OP2
(Lane28~31)

20180904
Add GND test point to RMS Jitter measure



(38) PEX_CLK_100M_PCIE_P
(38) PEX_CLK_100M_PCIE_N

PEX 8724

Station 0

PEX 8724

Station 1

<Variant Name>

ufiSpace

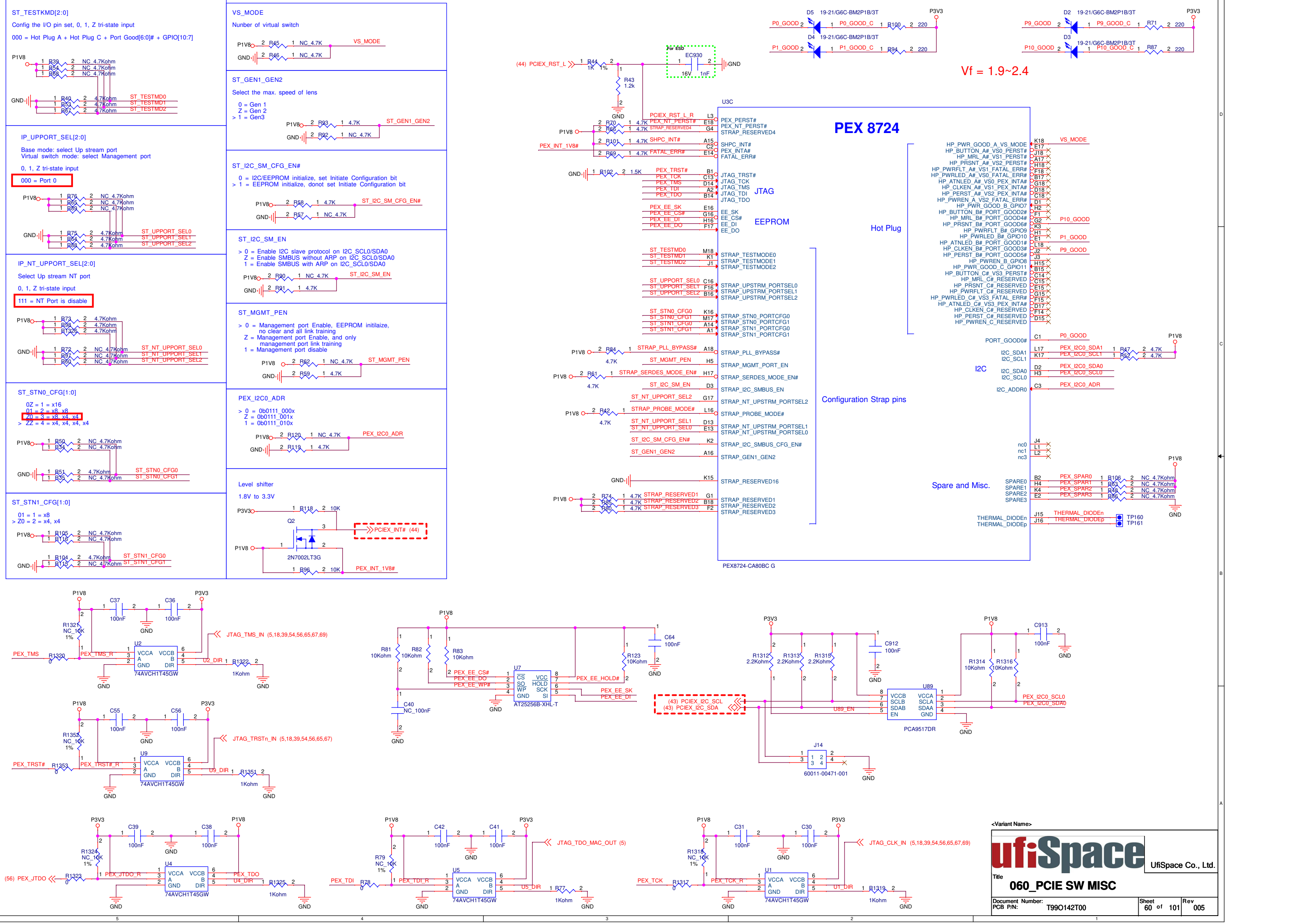
UfiSpace Co., Ltd.

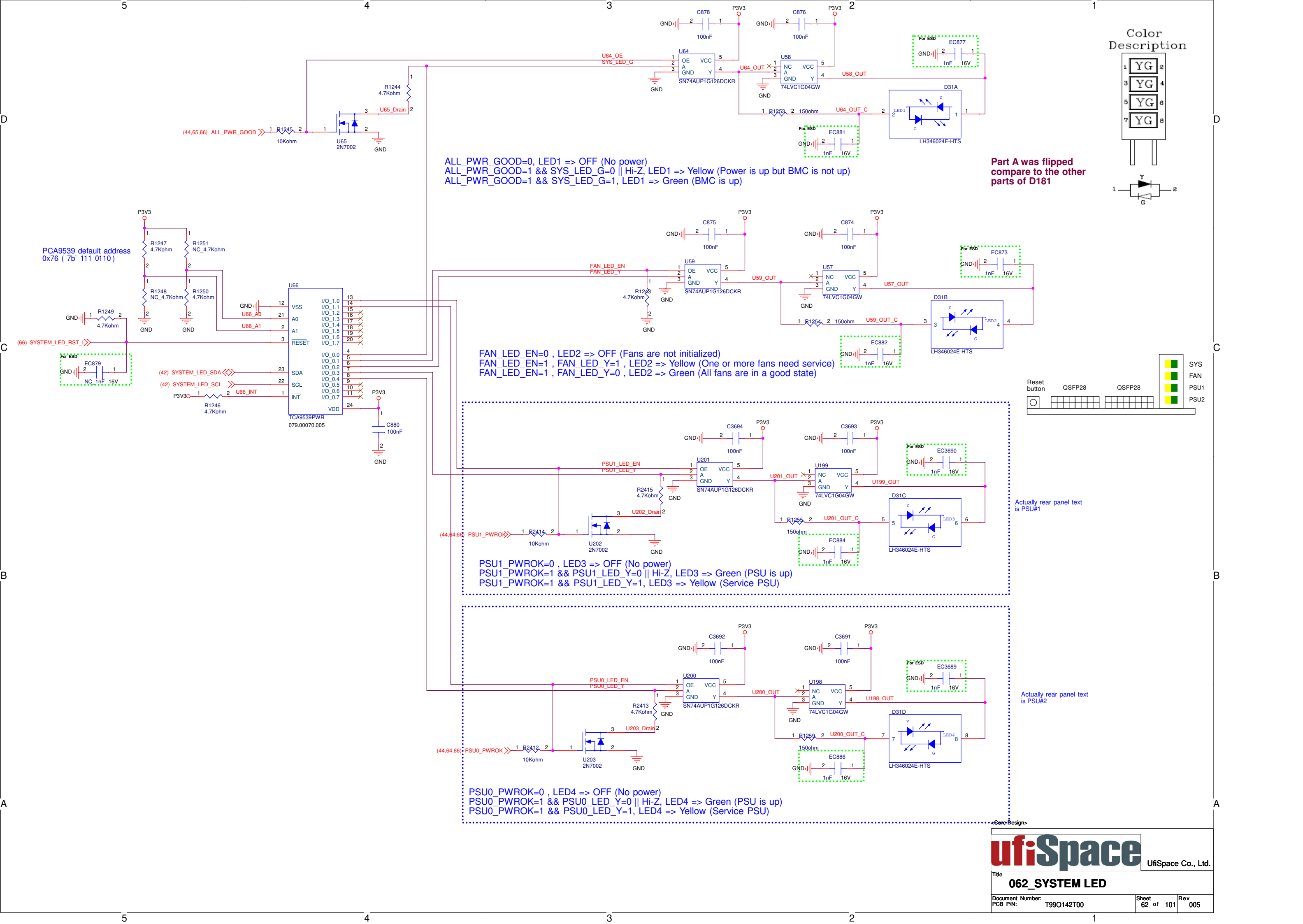
Title
059_PCIE SW SerDes

Document Number:
PCB P/N: T99O142T00

Sheet
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005

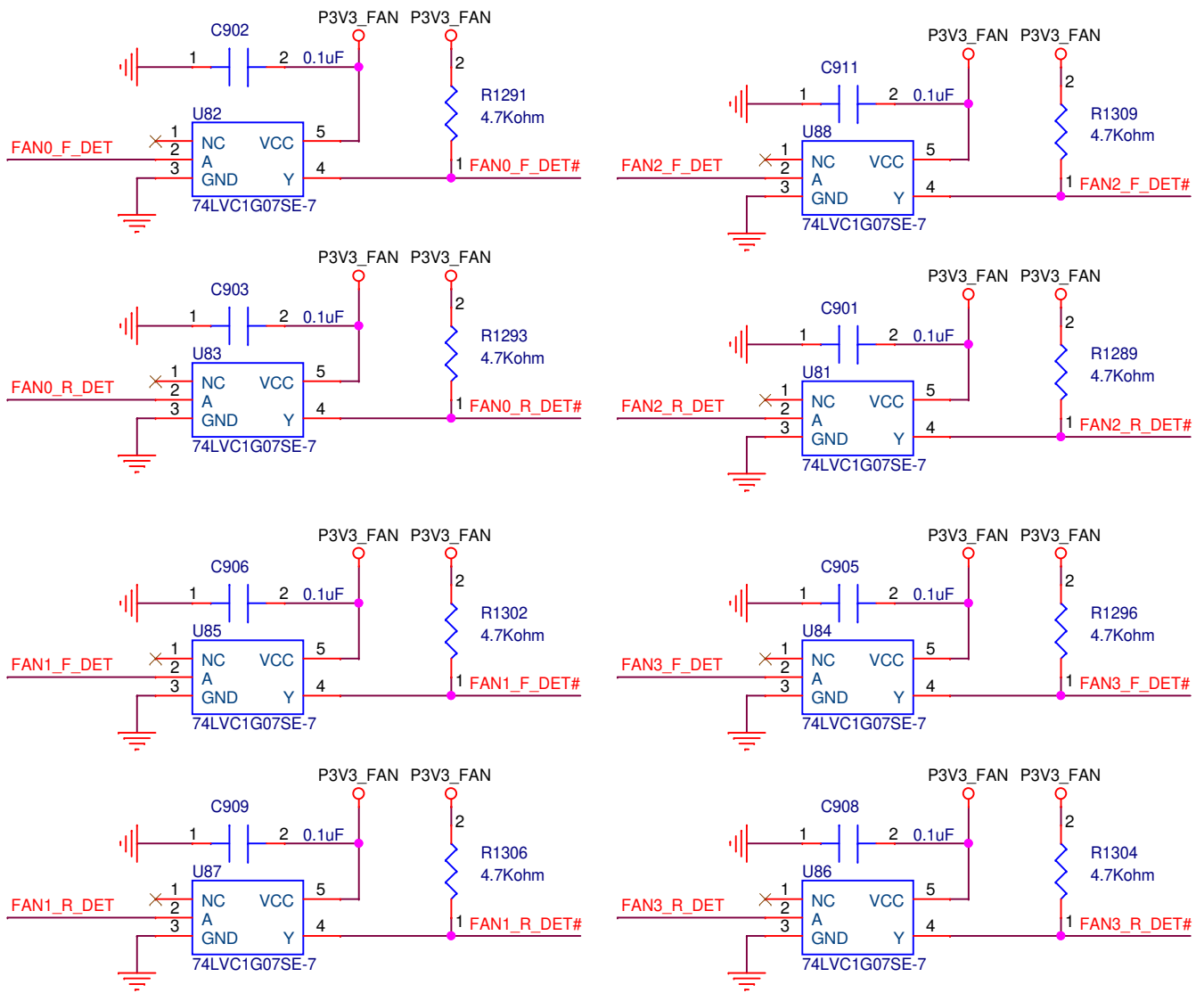
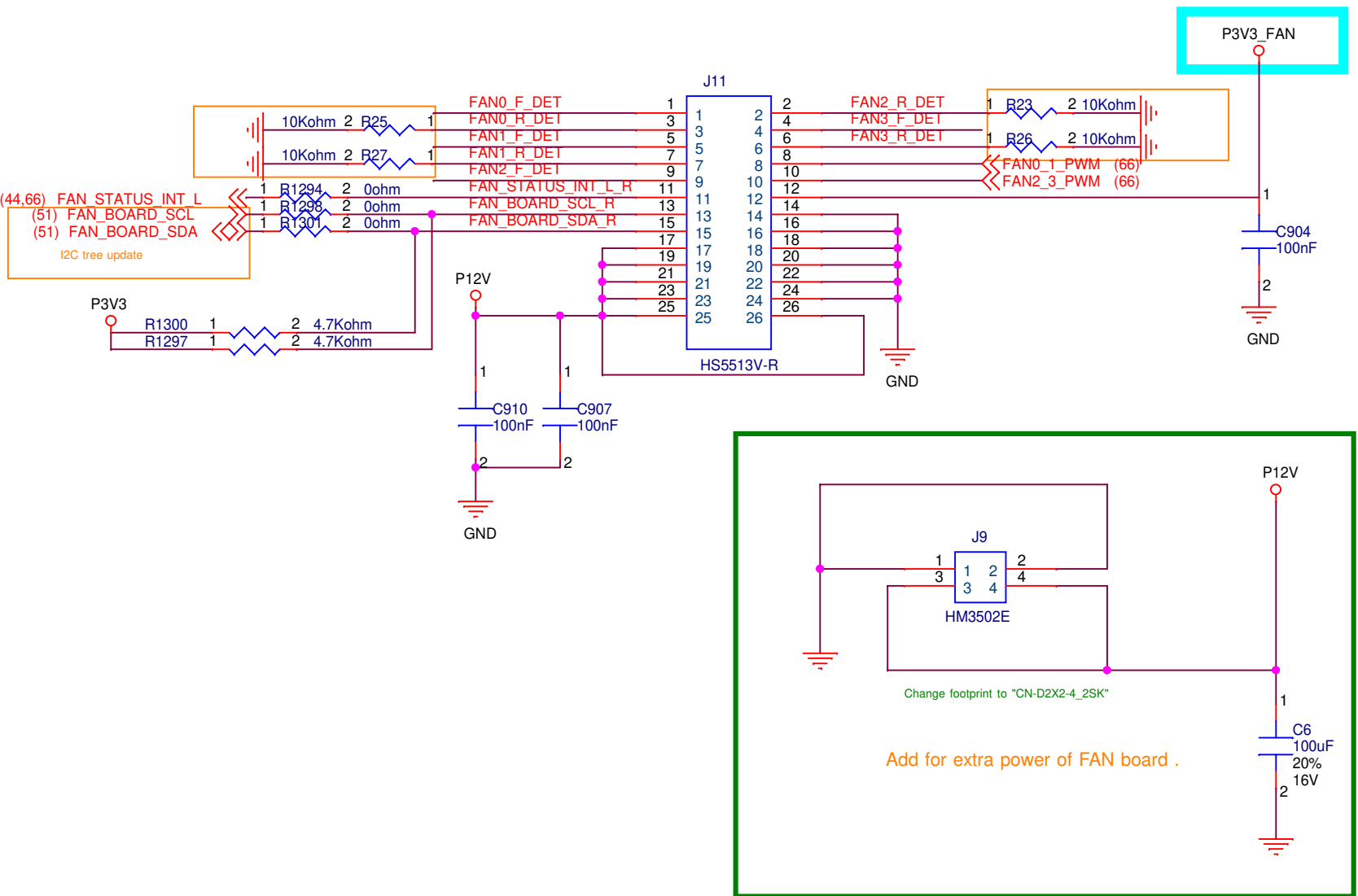




Changed all power source from P3V3 to P3V3_FAN.

TO FAN BOARD CONNECTOR

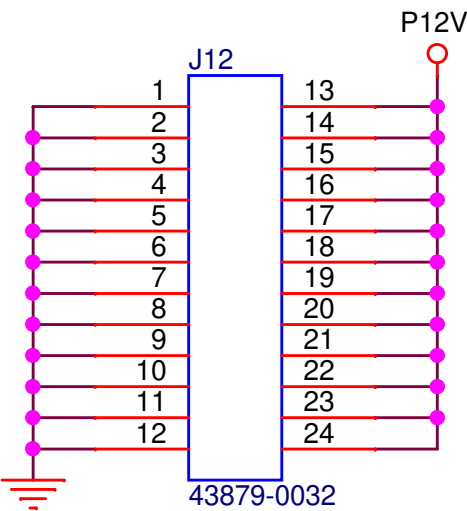
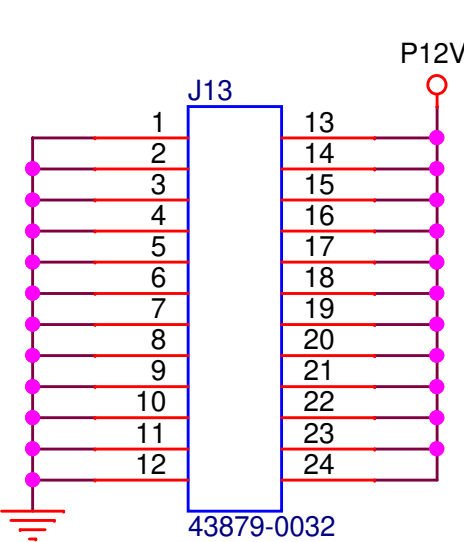
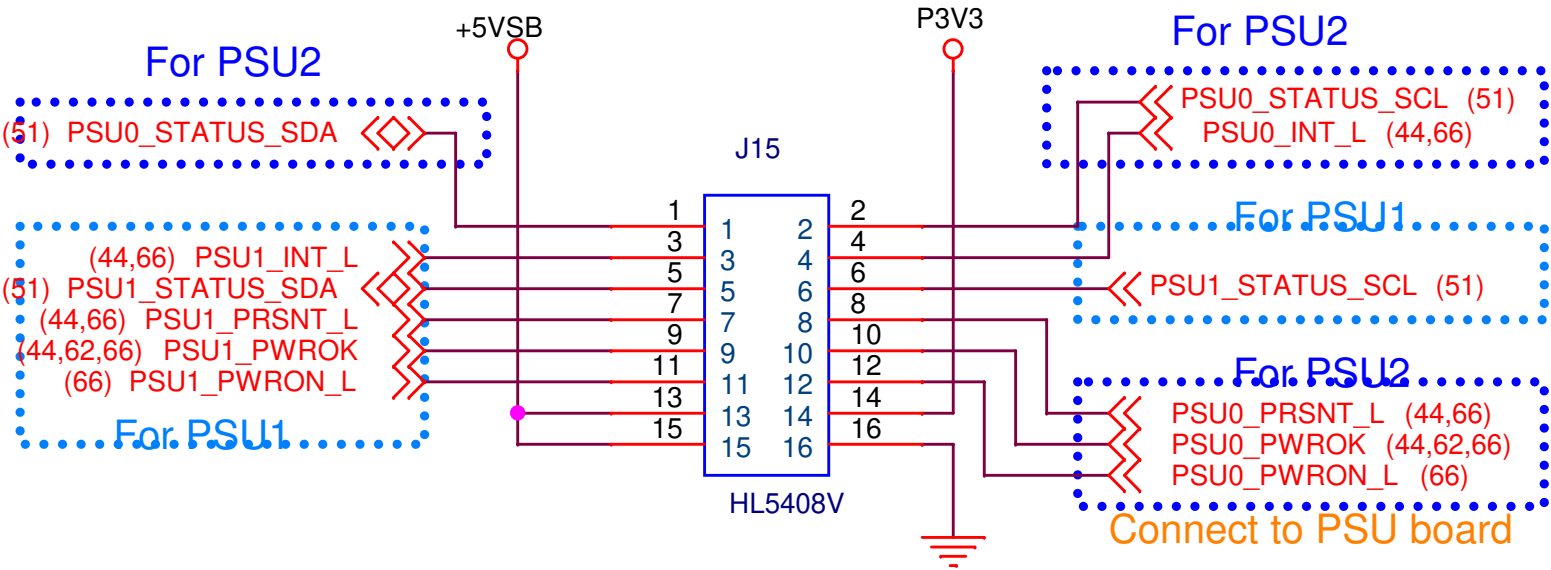
- (66) HWM_FAN0_F_DET << 1 R1292 2 0ohm FAN0_F_DET#
- (66) HWM_FAN0_R_DET << 1 R1295 2 0ohm FAN0_R_DET#
- (66) HWM_FAN1_F_DET << 1 R1303 2 0ohm FAN1_F_DET#
- (66) HWM_FAN1_R_DET << 1 R1307 2 0ohm FAN1_R_DET#
- (66) HWM_FAN2_F_DET << 1 R1310 2 0ohm FAN2_F_DET#
- (66) HWM_FAN2_R_DET << 1 R1290 2 0ohm FAN2_R_DET#
- (66) HWM_FAN3_F_DET << 1 R1299 2 0ohm FAN3_F_DET#
- (66) HWM_FAN3_R_DET << 1 R1305 2 0ohm FAN3_R_DET#



POWER CONNECTOR

PSU CONNECTOR 0 (LEFT)
I2C ADDRESS 0x1010000X

PSU CONNECTOR 1 (RIGHT)
I2C ADDRESS 0x1010000X



<Core Design>

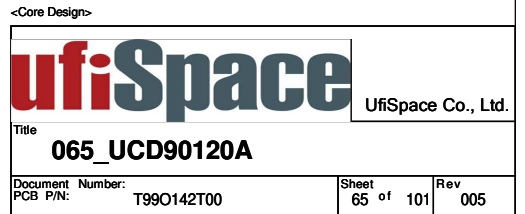


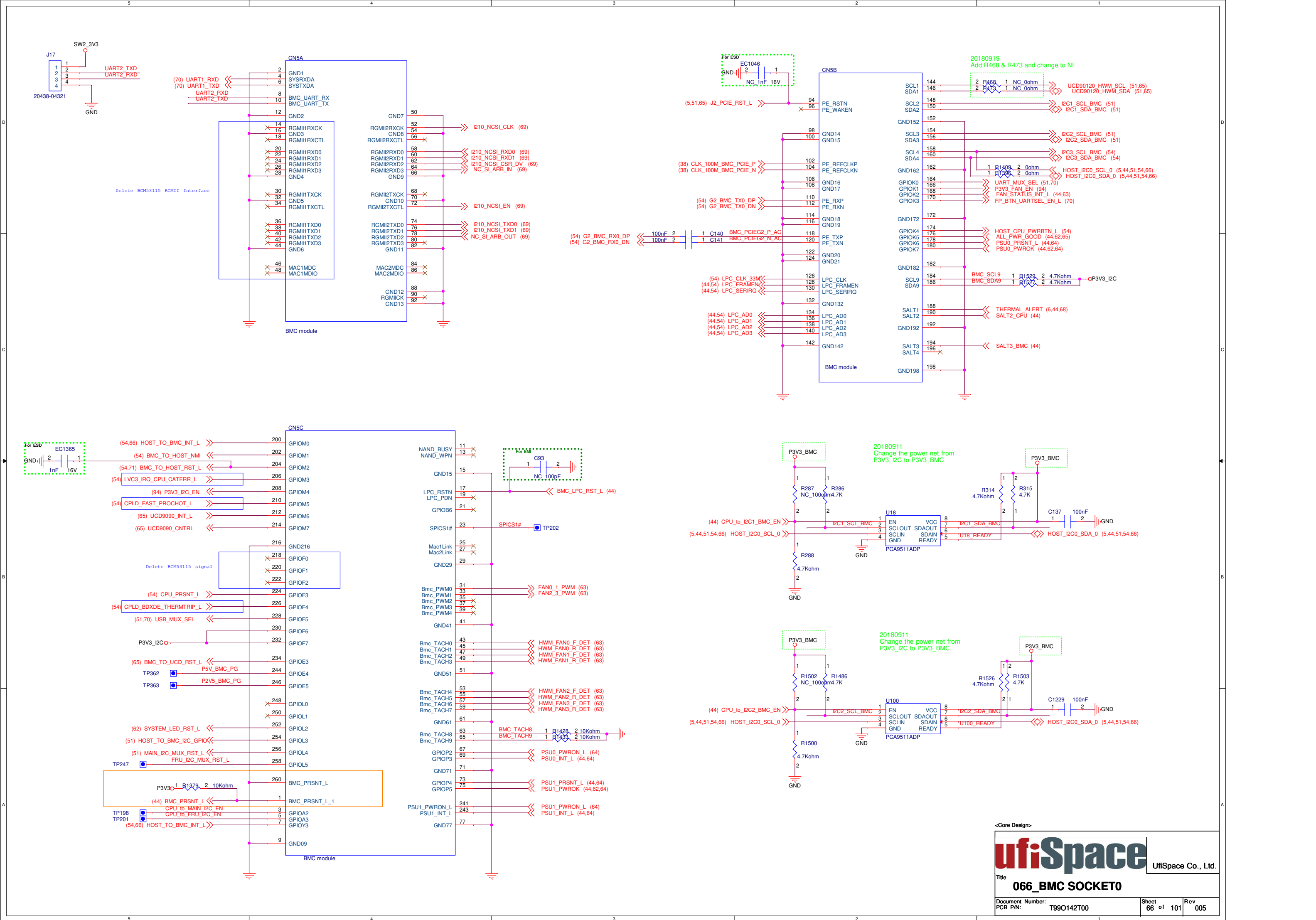
UfiSpace Co., Ltd.

Title
064_POWER CONNECTOR

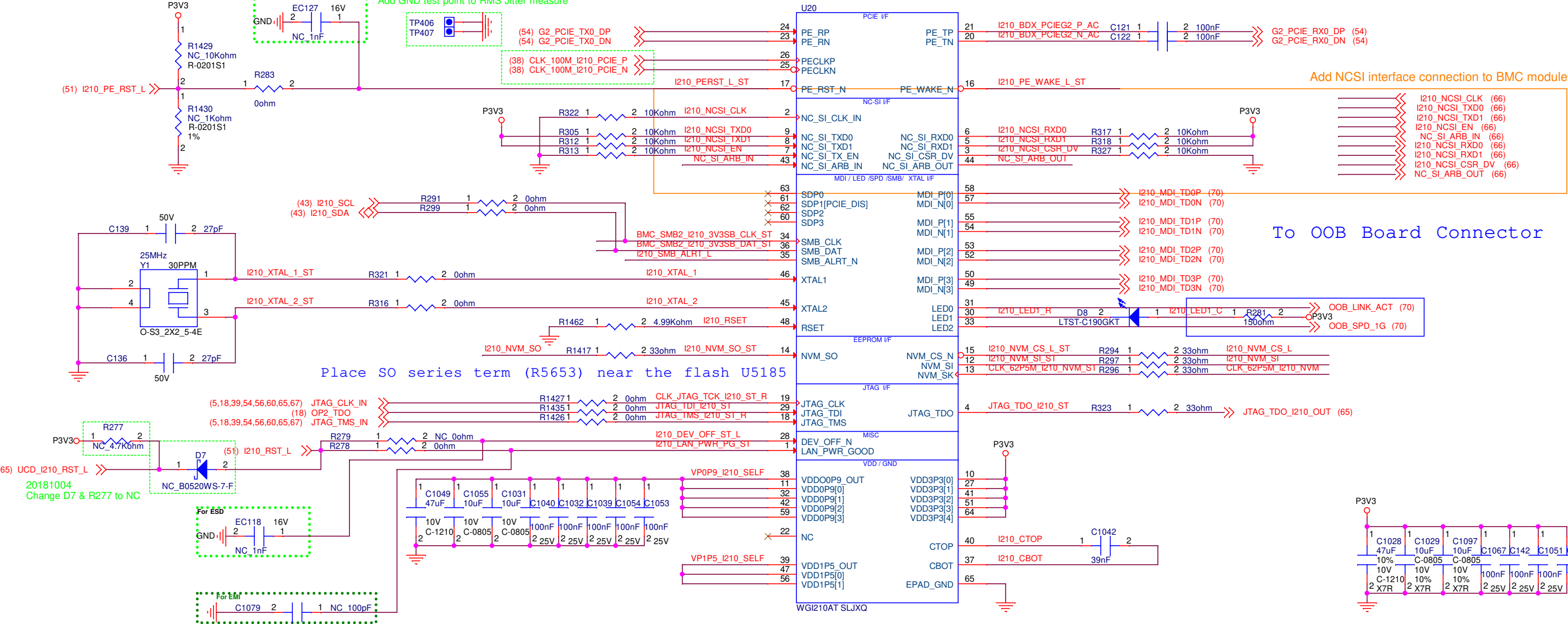
Document Number: PCB P/N: T99O142T00	Sheet 64 of 101	Rev 005
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Jericho-2:	OP2:
1. P3V3	1. P3V3
2. ROV_CORE	2. P0V9_VDDM
3. P0V8	3. P0V8_VDDSL
4. P1V8	0V8_CORE
5. P1V2_3	AVS_CORE
6. P0V88	4. P1V8
7. P2V5	P1V2_3
8. P1V2_1	
9. P1V2_2	
10. SYS_RST_N	
11. PCIE_RST	



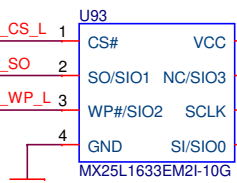


For ESD



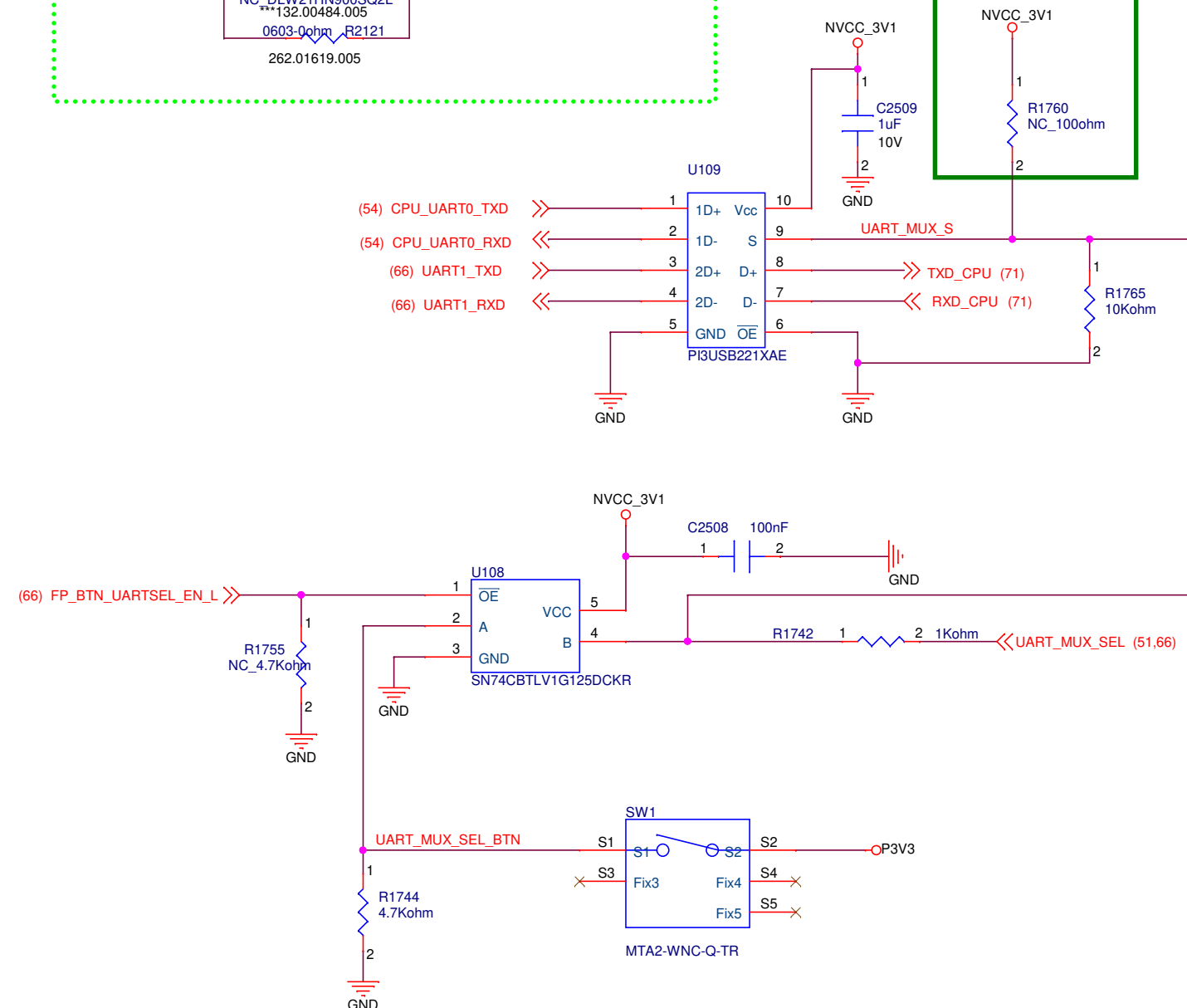
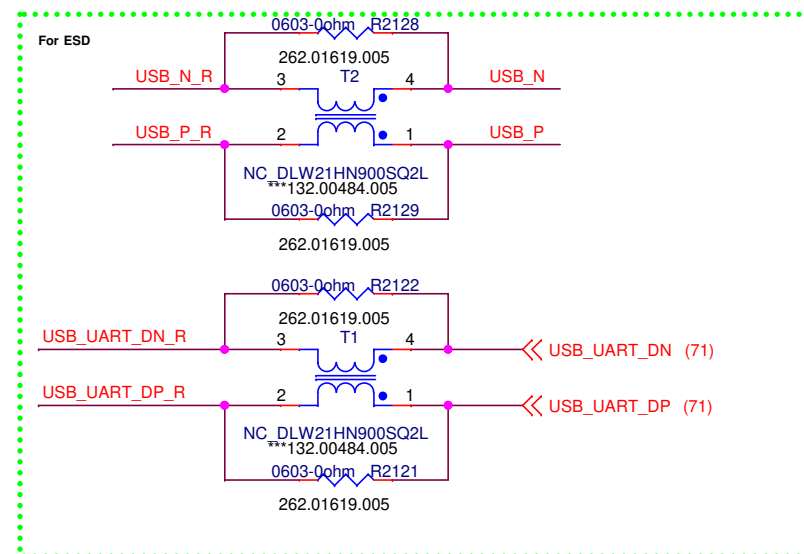
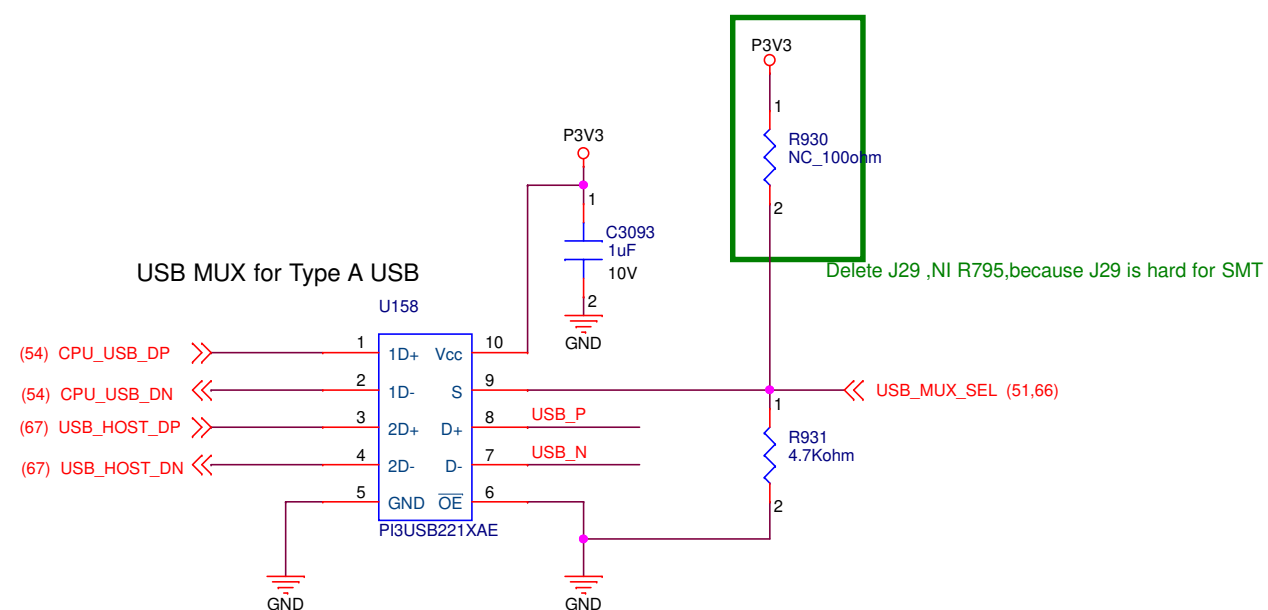
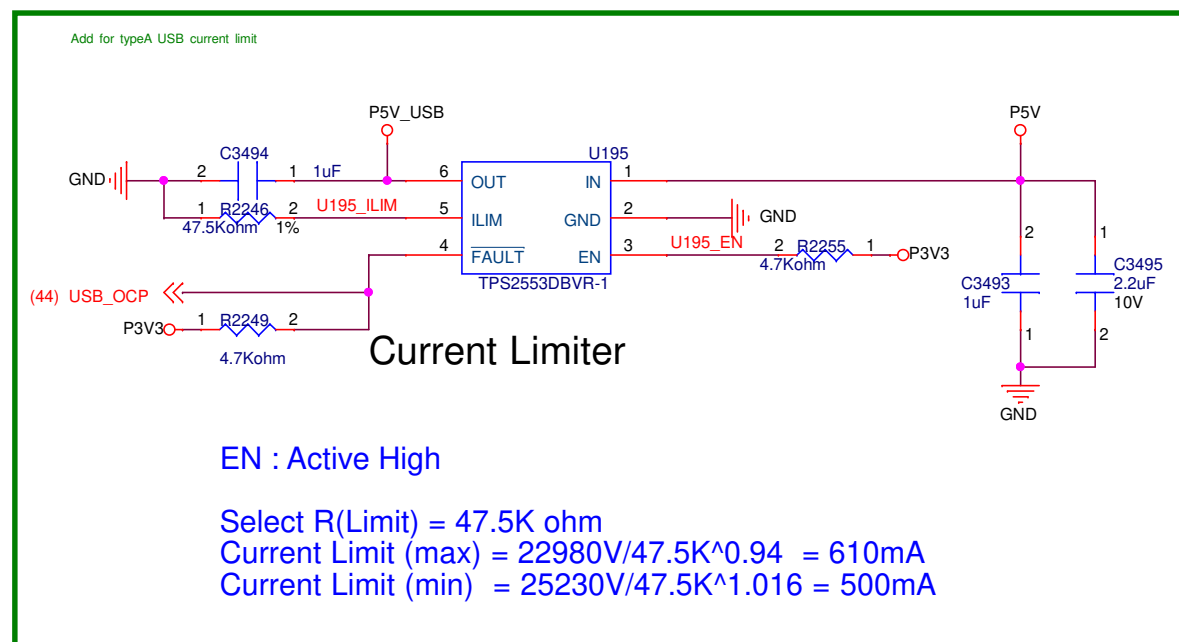
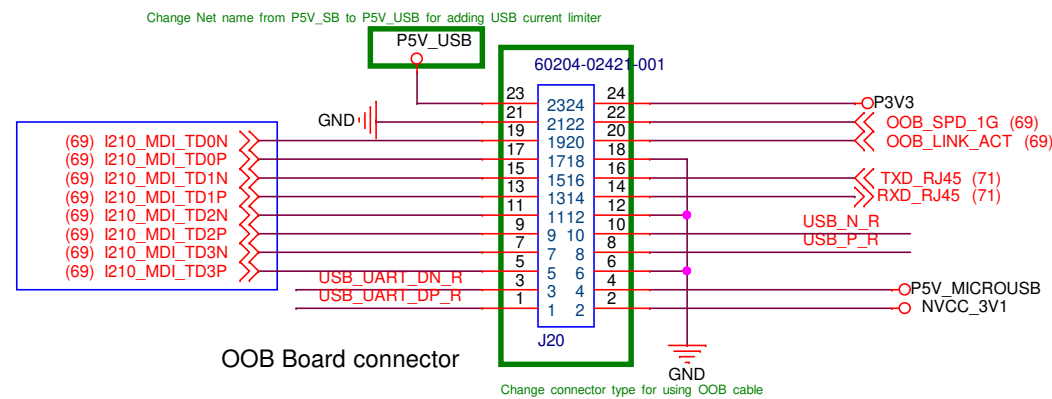
Based on checklist rev2.1: If a Flash is not used add a 3.3Kohm pull-up to NVM_S0

NVM 16Mb

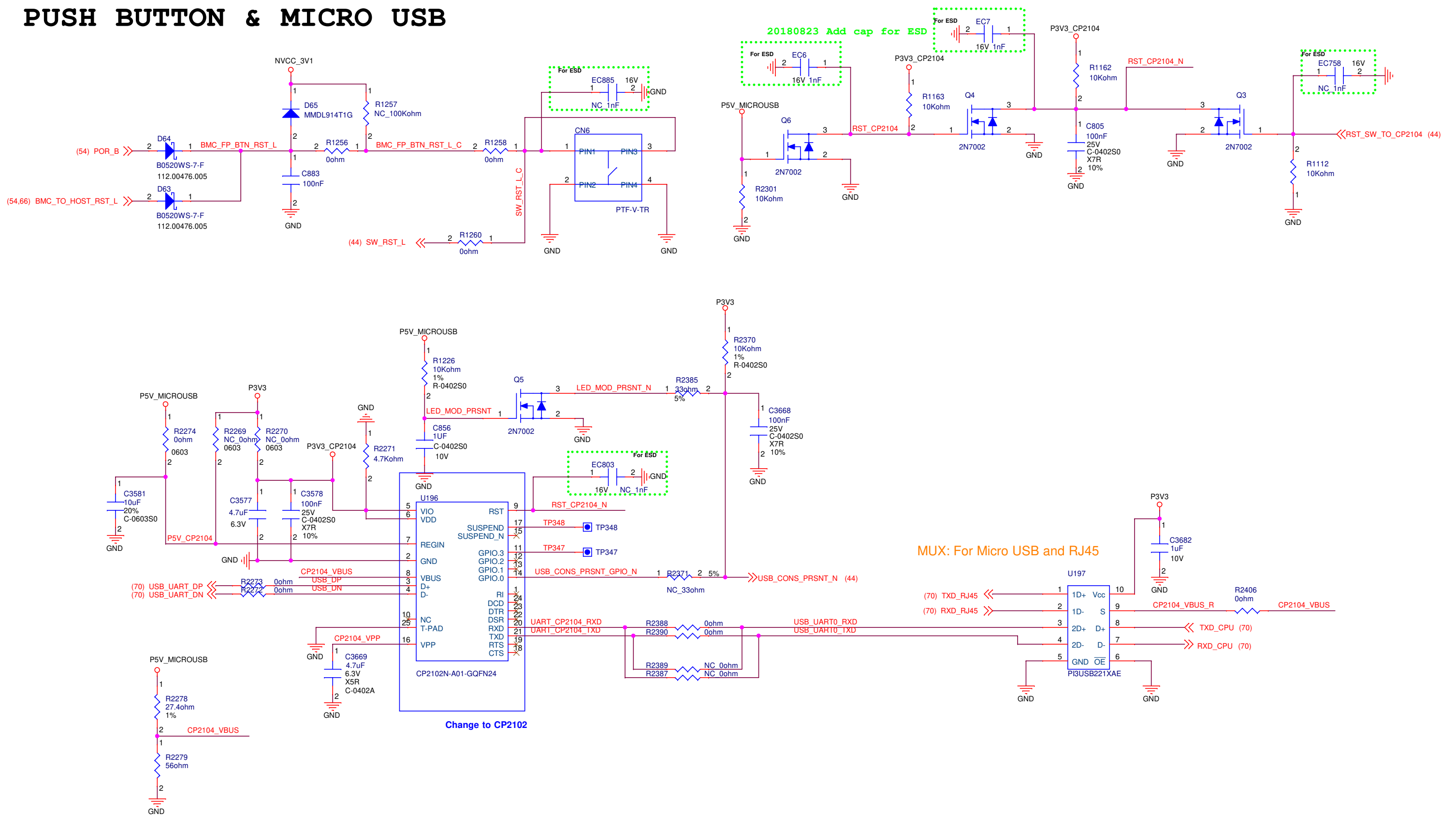


		UfiSpace Co., Ltd.	
Title 069_ETH CONTROLLER WGI210AT			
Document Number: PCB P/N: T99O142T00		Sheet 69 of 101	Rev 005

OOB PORT RJ-45 + Console Connector



PUSH BUTTON & MICRO USB



<Core Design>

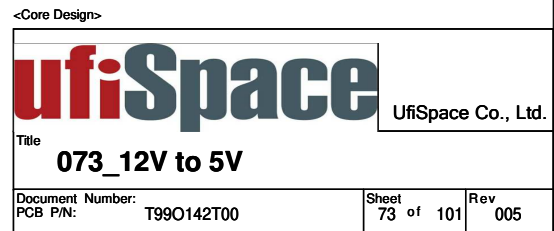
ufiSpace UfiSpace Co., Ltd.

Title	071 PUSH BUTTON & MICRO USB
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Document Number: PCB P/N: T99O142T00	Sheet 71 of 101	Rev 005
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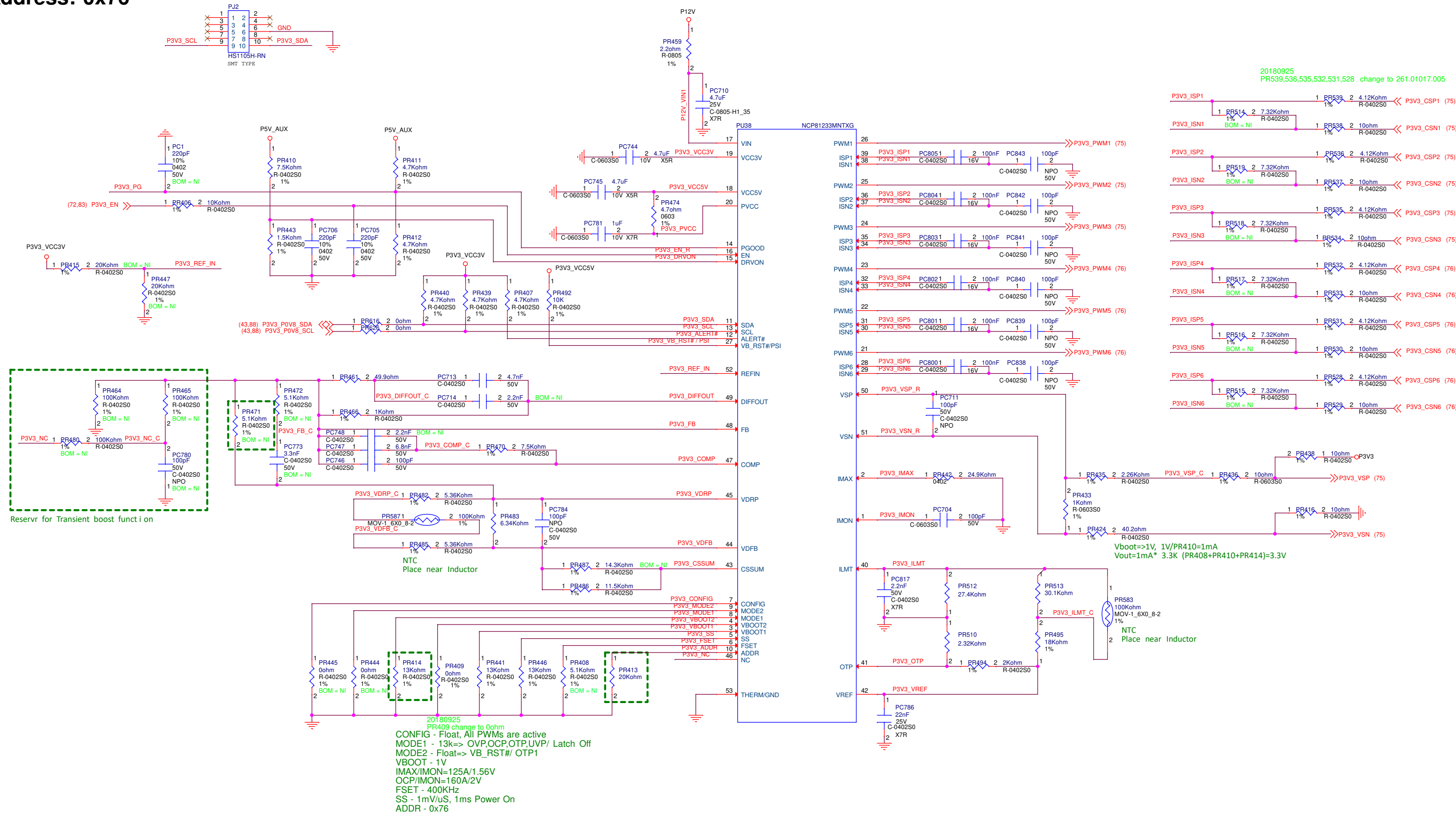
			UfiSpace Co., Ltd.		
Title 072_SYSTEM PWR Sequence					
Document Number: PCB P/N: T99O142T00			Sheet 72 of 101		Rev 005

P5V_AUX/4A



3.3V/120A controller

Address: 0x76



ufiSpace

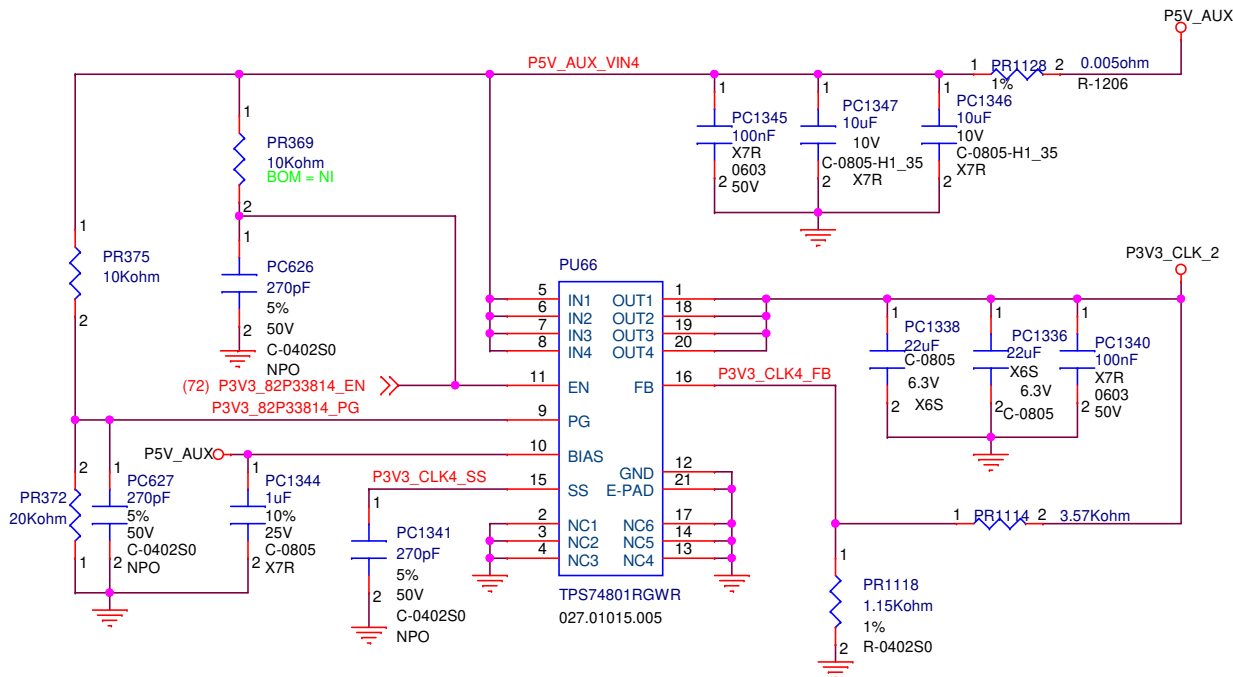
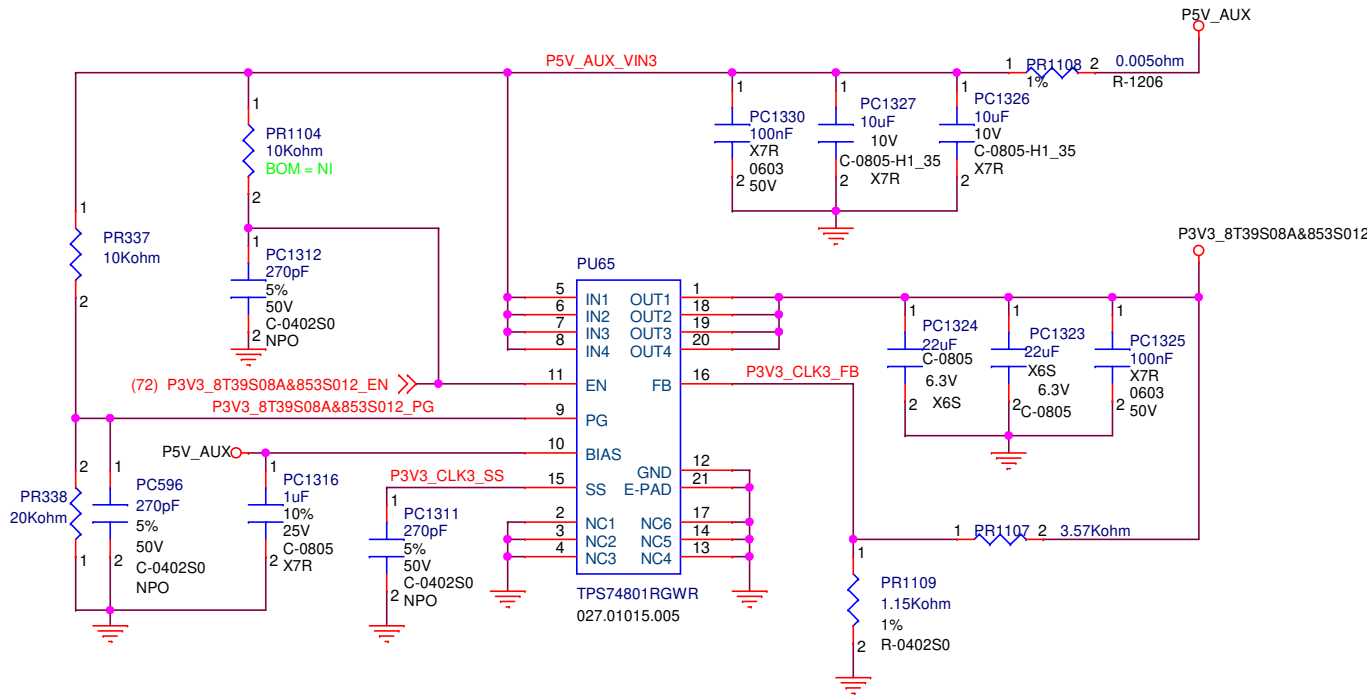
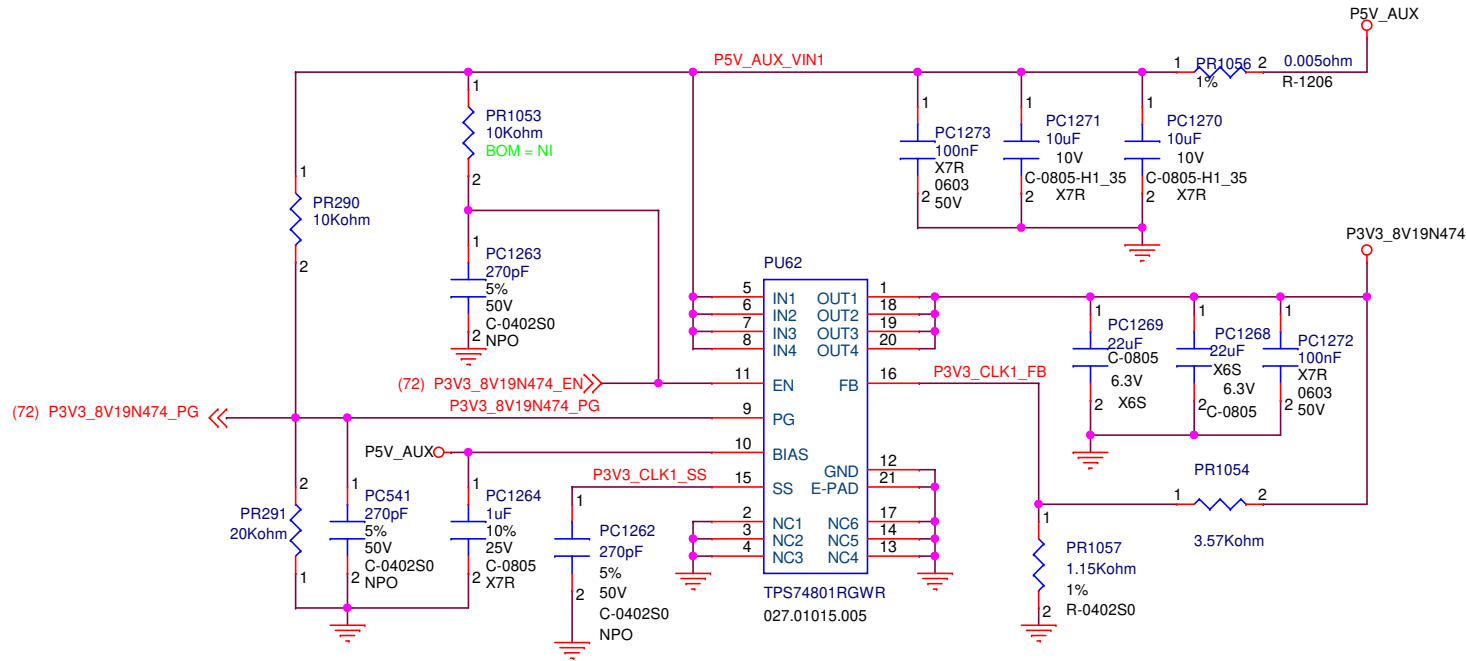
ufiSpace Co., Ltd.

Title

076_12V to 3V3/125A_4-6

Document PCB P/N:	Number: T99O142T00	Sheet 76 of 101	Rev 005
----------------------	-----------------------	--------------------	------------

P3V3_CLK



<Variant Name>



UfiSpace Co., Ltd.

Title

077_5V to 3V3_CLK

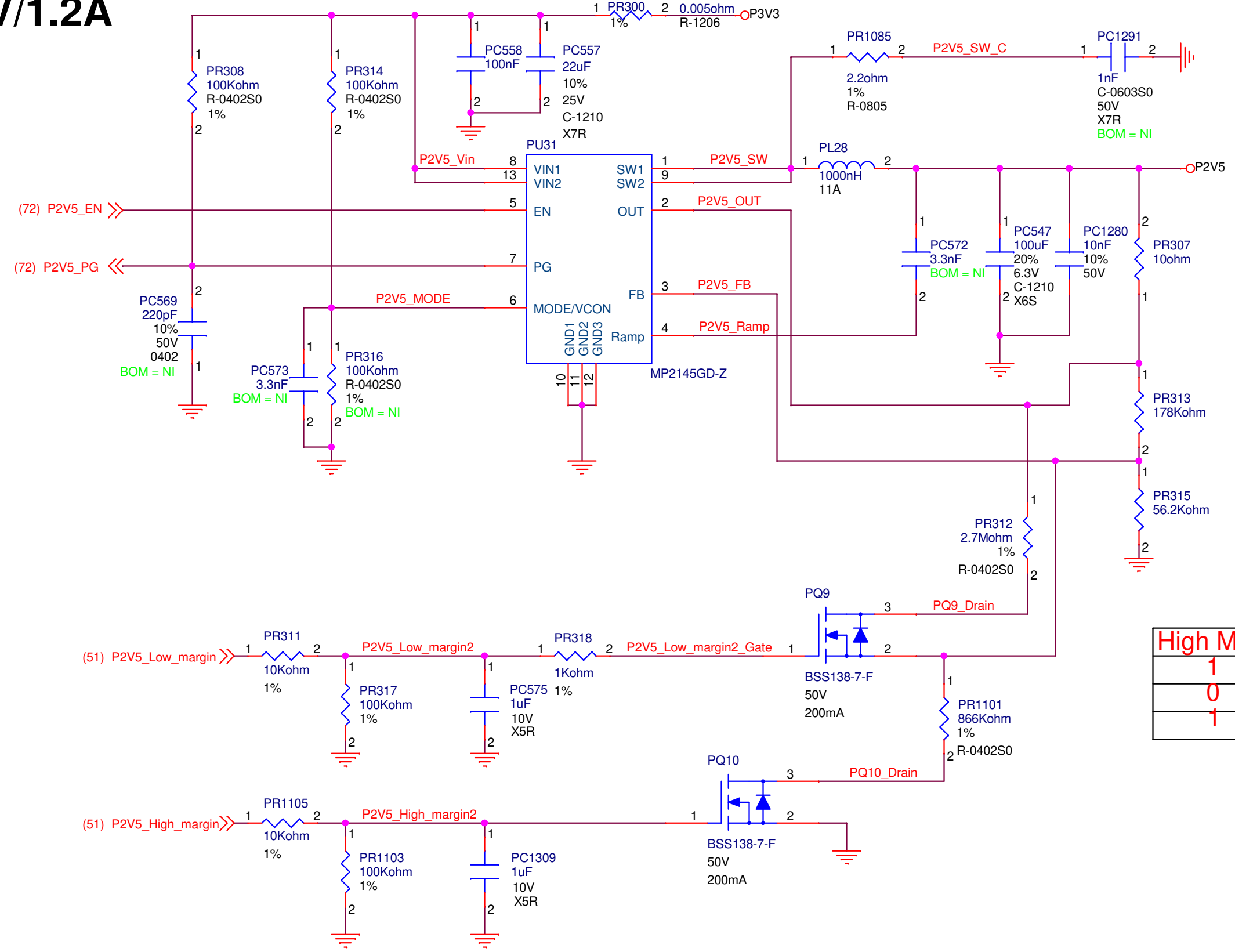
Document Number: T990142T00

PCB P/N:

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Rev 005

2.5V/1.2A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

ufiSpace

UfiSpace Co., Ltd.

Title

078_3V3 to 2.5V/1.2A

Document Number:

T99O142T00

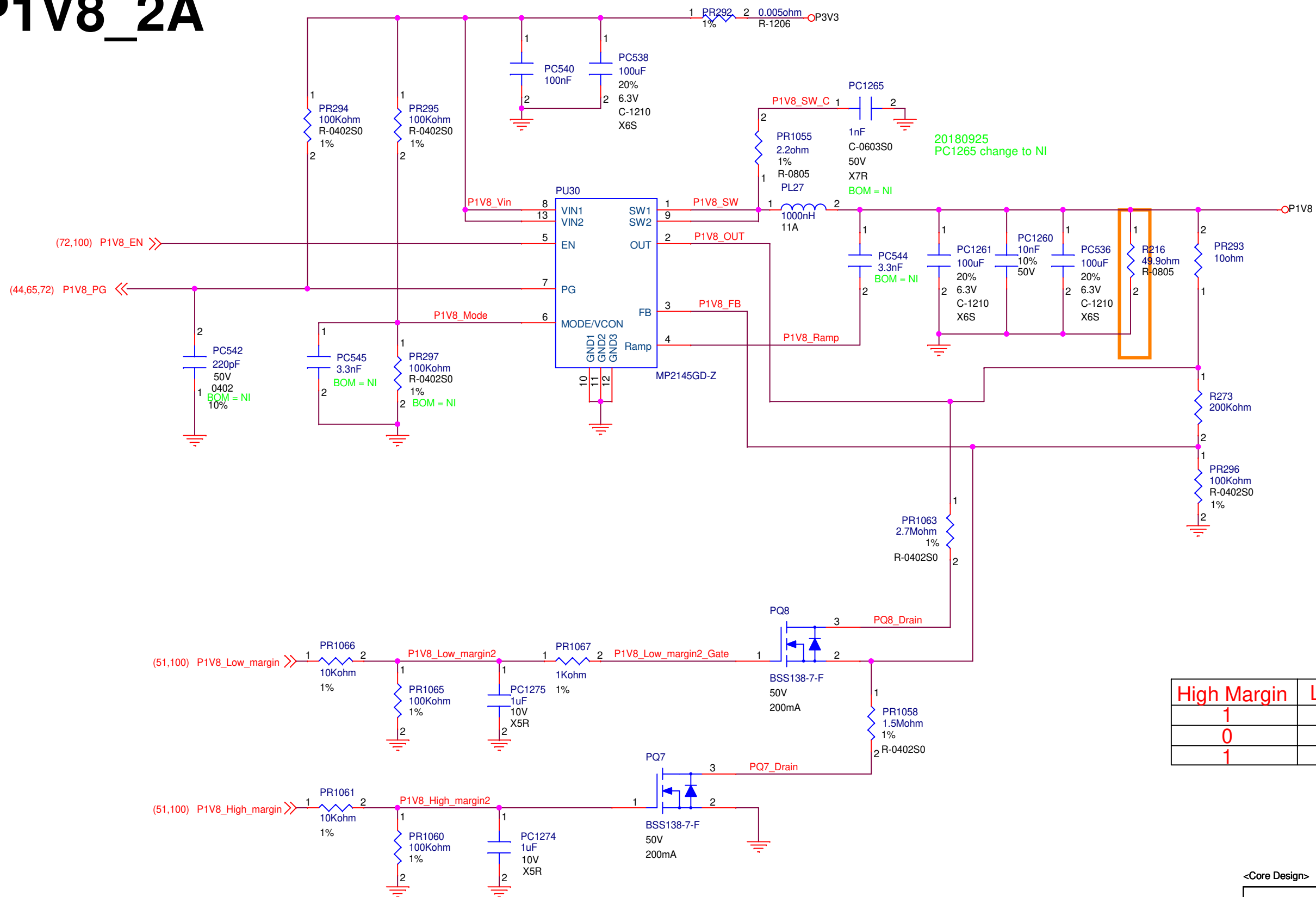
Sheet

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Rev

005

P1V8_2A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	$0.95V_o$
1	0	$1.05V_o$

<Core Design>



UfiSpace Co., Ltd.

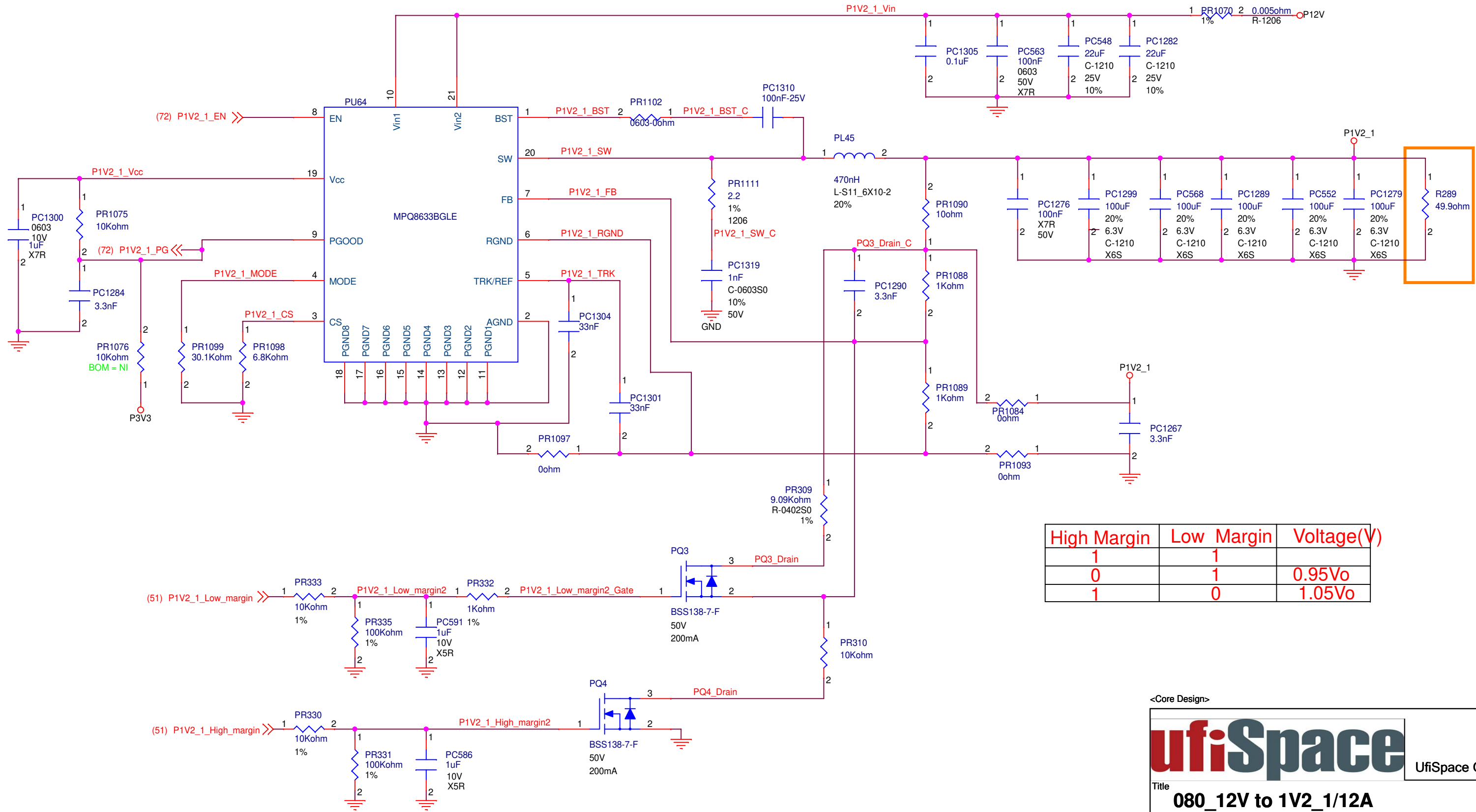
Title

079_3V3 to 1V8/2A

Document Number:
PCB P/N: T99O142T00

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--------------------	------------

P1V2_1/12A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>

ufiSpace

UfiSpace Co., Ltd.

Title

080_12V to 1V2_1/12A

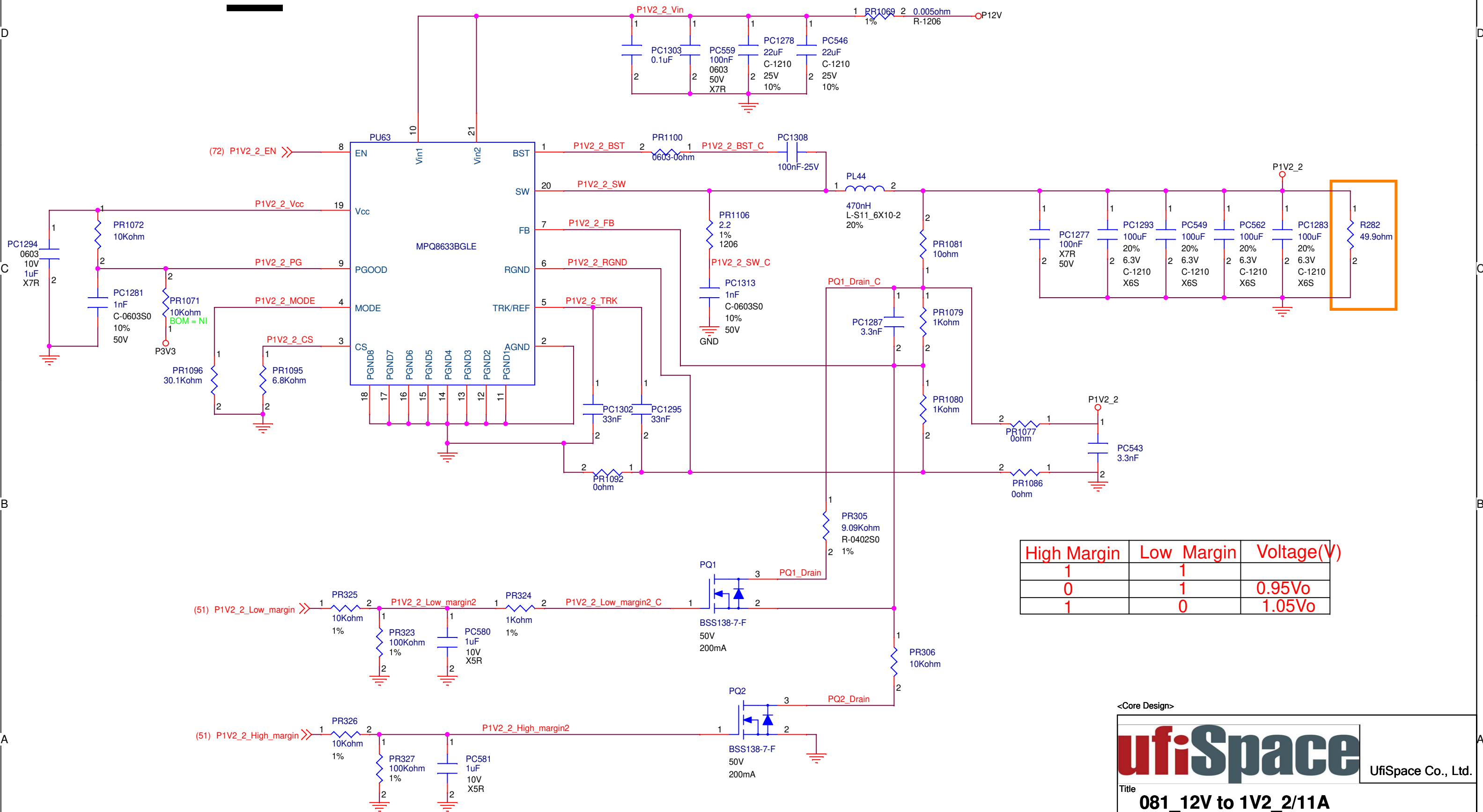
Document Number: T99O142T00

PCB P/N:

Sheet 80 of 101

Rev 005

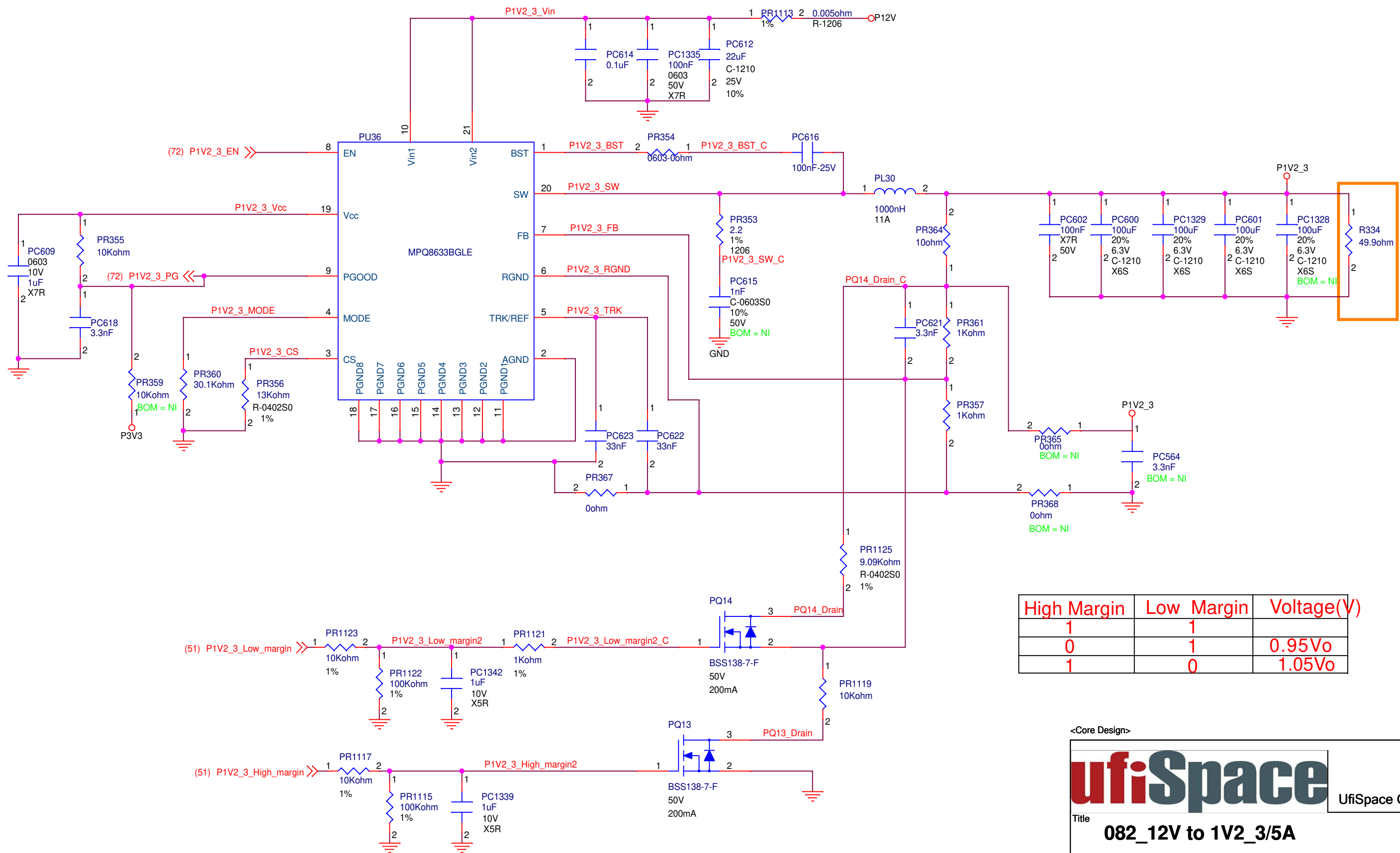
P1V2_2/11A



<Core Design>

		UfiSpace Co., Ltd.	
Title			
081_12V to 1V2_2/11A			
Document Number:		Sheet	Rev
PCB P/N: T99O142T00		81 of 101	005

P1V2_3/5A



<Core Design>

ufiSpace

UfiSpace Co., Ltd.

Title

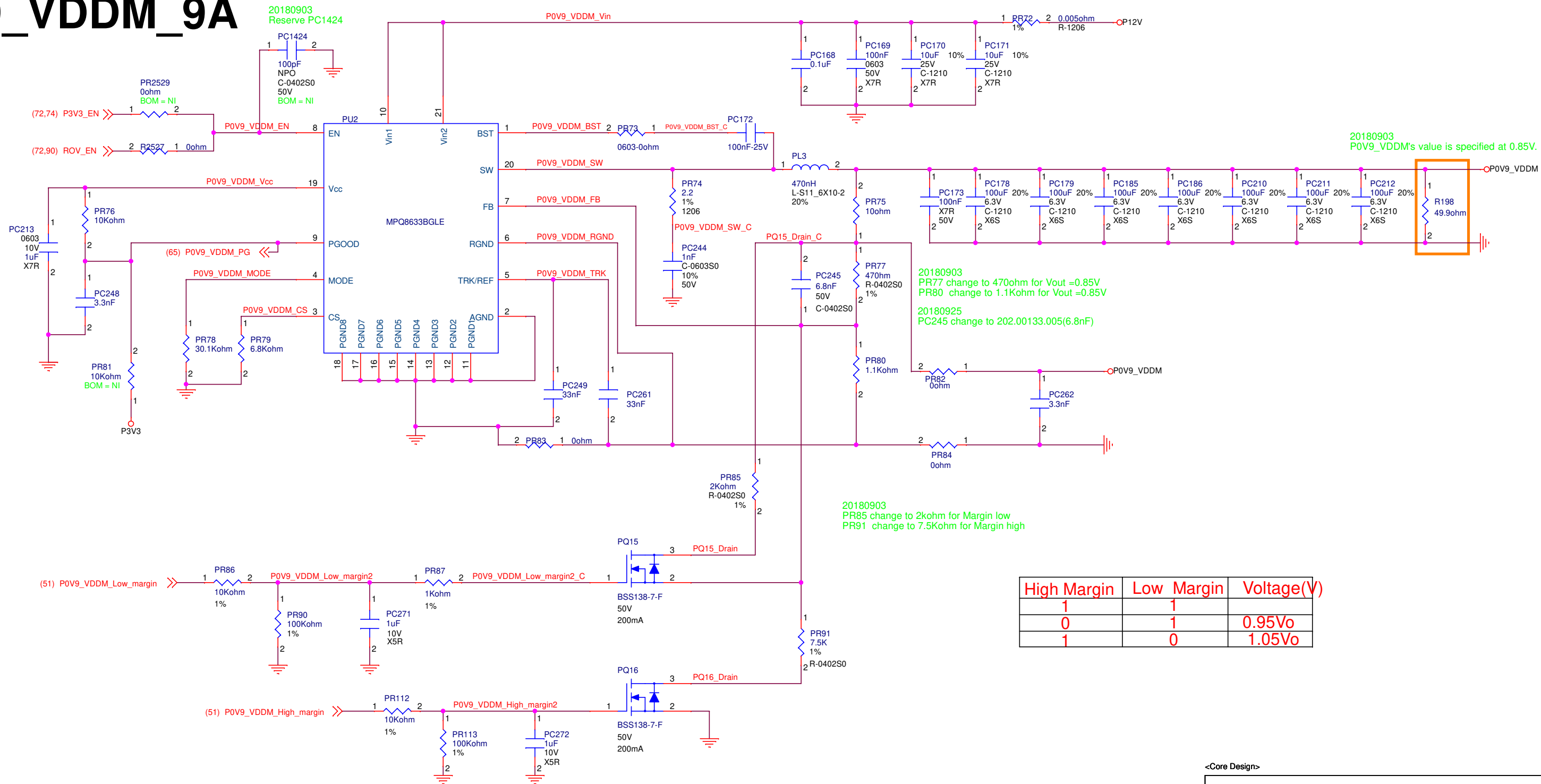
082_12V to 1V2_3/5A

Document Number: T99O142T00

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Rev 005

P0V9_VDDM_9A



VDDM powers the SRAM on the chip.
Its value is specified at 0.85V. A separate power supply is required for VDDM as it is a different voltage from VDD or the analog supplies.
Due to the high current requirement, a switching regulator is recommended to power VDDM.

<Core Design>

ufiSpace UfiSpace Co., Ltd.

Title
083_12V to 0.9V_VDDM/9A

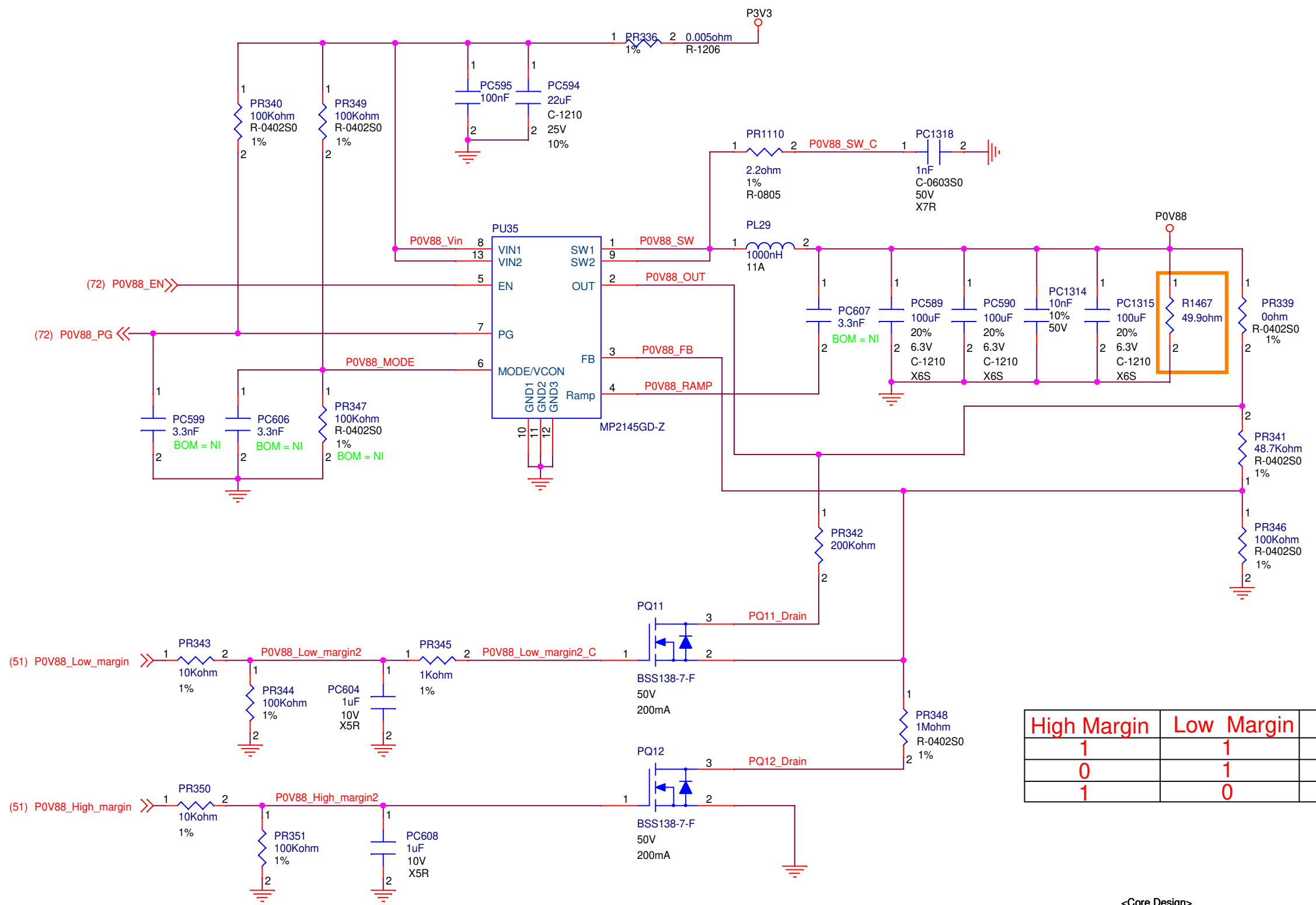
Document Number: T99O142T00

PCB P/N: T99O142T00

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Rev 005

P0V88_4A



<Core Design>



UfiSpace Co., Ltd.

Title

084_3V3 to 0V88/4A

Document Number:

T99O142T00

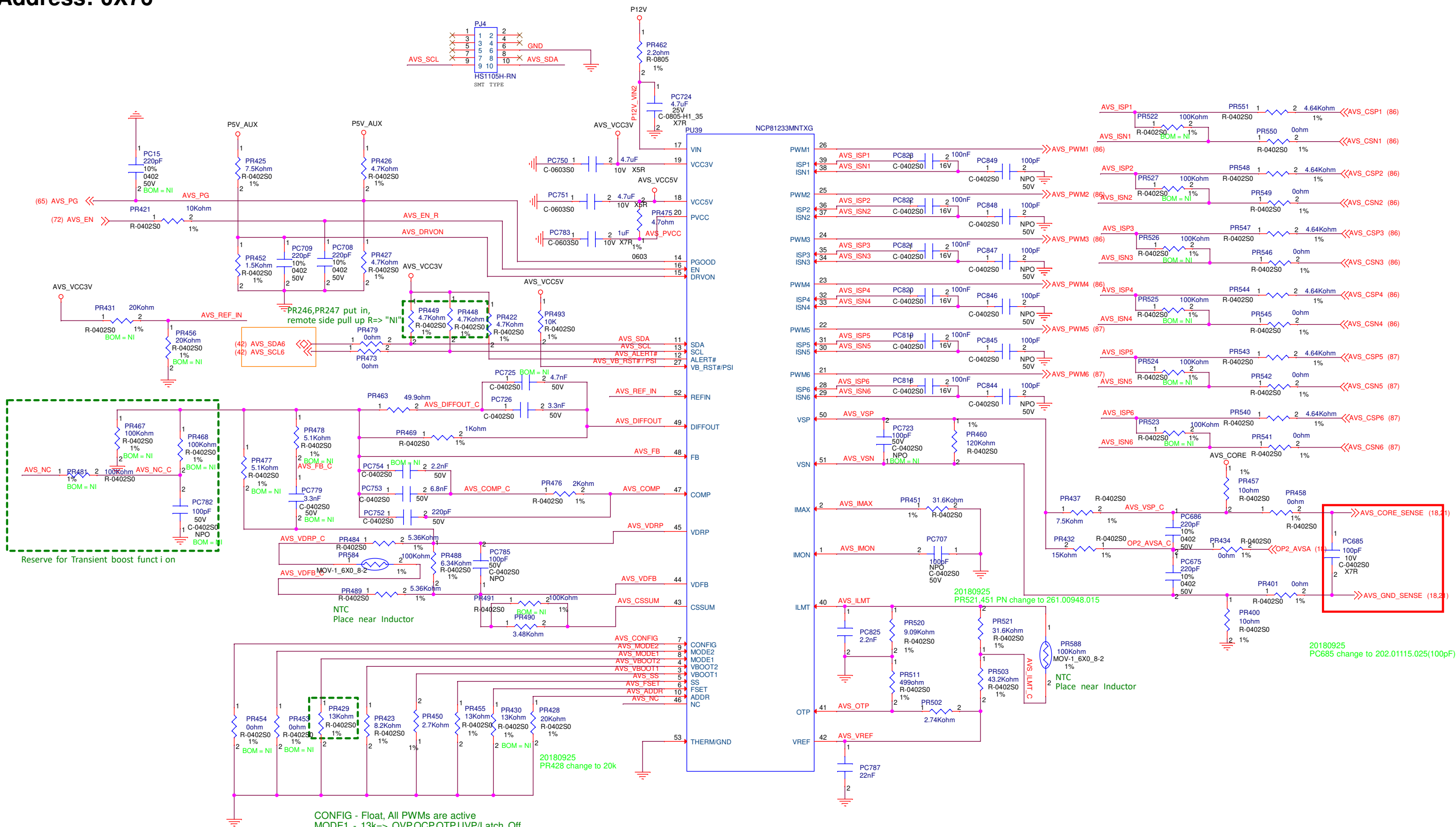
Sheet

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Rev

005

Address: 0X76



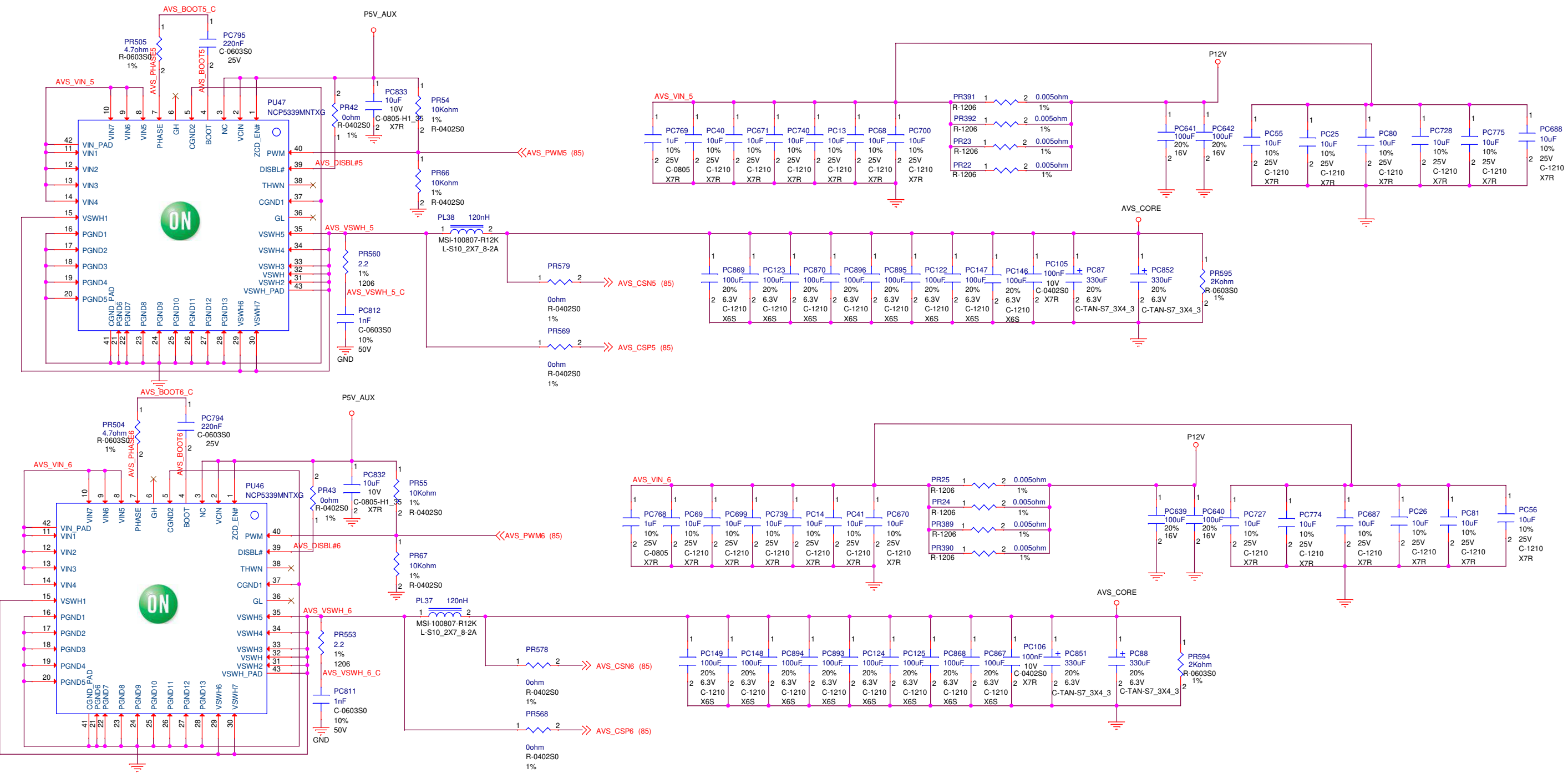
```

CONFIG - Float, All PWMs are active
MODE1 - 13k=> OVP,OCP,OTP,UVP/Latch Off
MODE2 - Float=> VB_RST# / OTP1
VBOOT - 0.8V,output voltage:0.85V=0.8*(1+7.5/120)
IMAX/IMON=150A/1.5V
OCP/IMON=200A/2V
FSET =>400KHz
SS - 1mV/uS, 0.8ms Power On
ADDR - 0X75

```

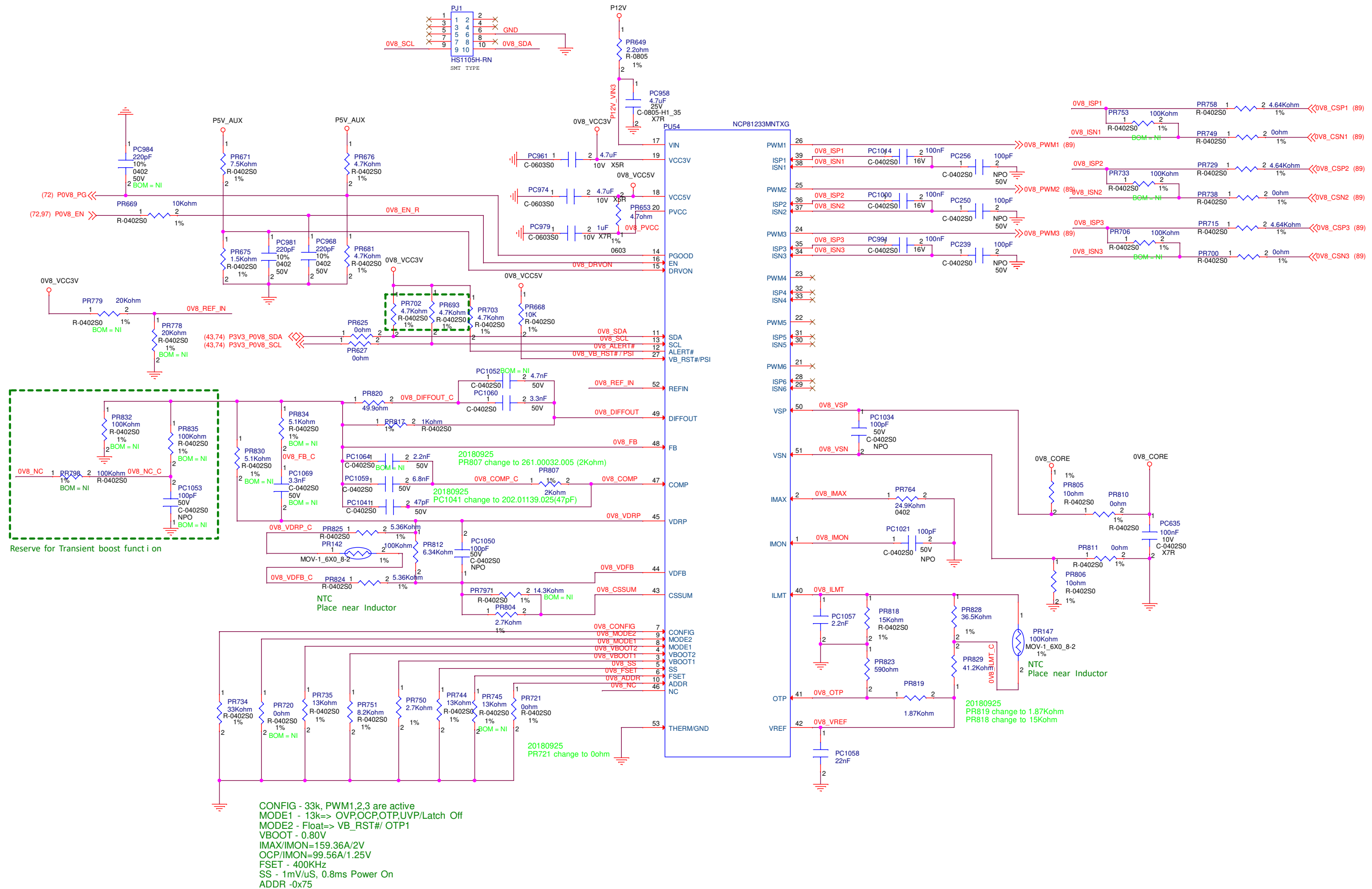
		UfiSpace Co., Ltd.	
Title			
086_12V to AVS_0.85V/150A_1-4			
Document Number: PCB P/N:	T990142T00	Sheet 86 of 101	Rev 005

AVS_0.85V /150A_Phase5~6



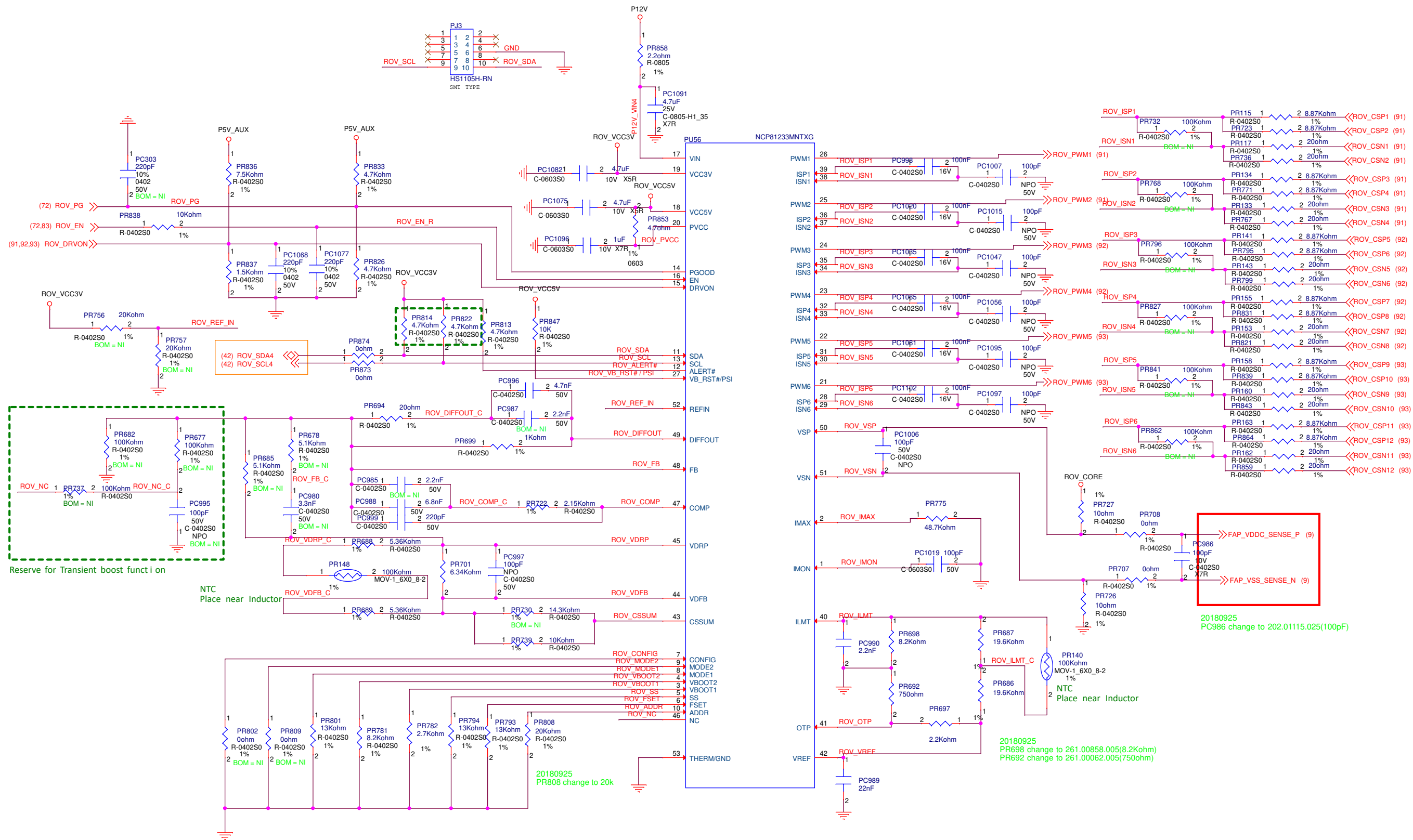
0.80V /97A_controller

Address:0x75



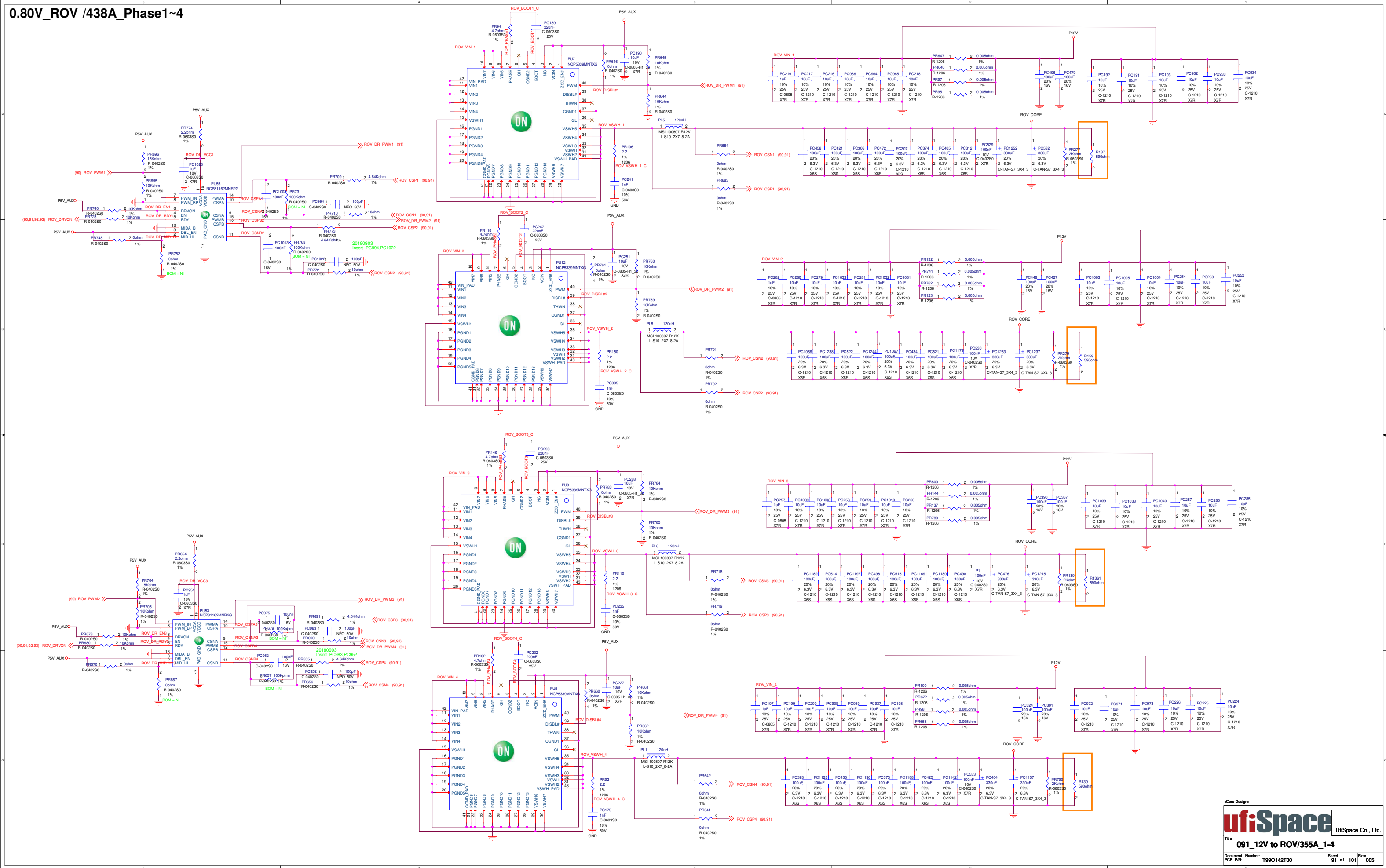
		Title 089_12V to 0V8/207A_1-4		UfiSpace Co., Ltd.	
Document PCB P/N:	Number: T99O142T00	Sheet 89 of 101	Rev 005		

0.80V_ROV /438A_Controller

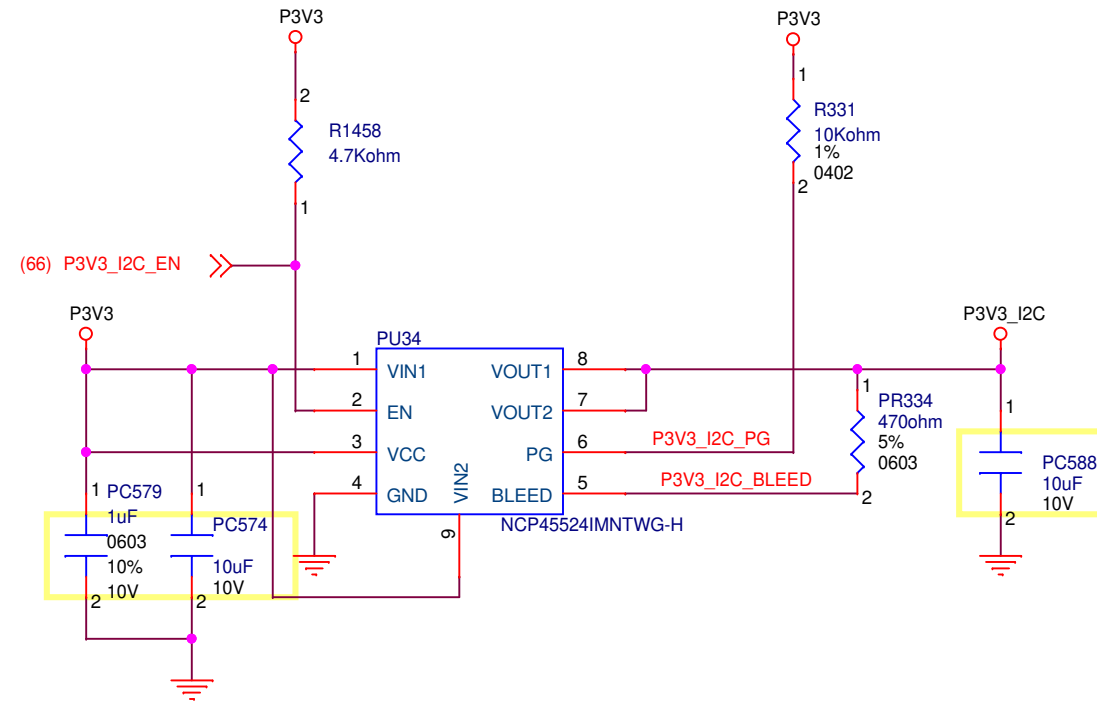


```
CONFIG - Float, All PWMs are active
MODE1 - 13k=> OVP,OCP,OTP,UVP/Latch Off
MODE2 - Float=> VB_RST#/ OTP1
VBOOT - 0.80V
IMAX/IMON=437A/1.52V
OCP/IMON=574A/2V
FSET - 800KHz / 2=>400KHz
SS - 1mV/uS, 0.8ms Power On
ADDR - 0x76
```

0.80V_ROV /438A_Phase1~4



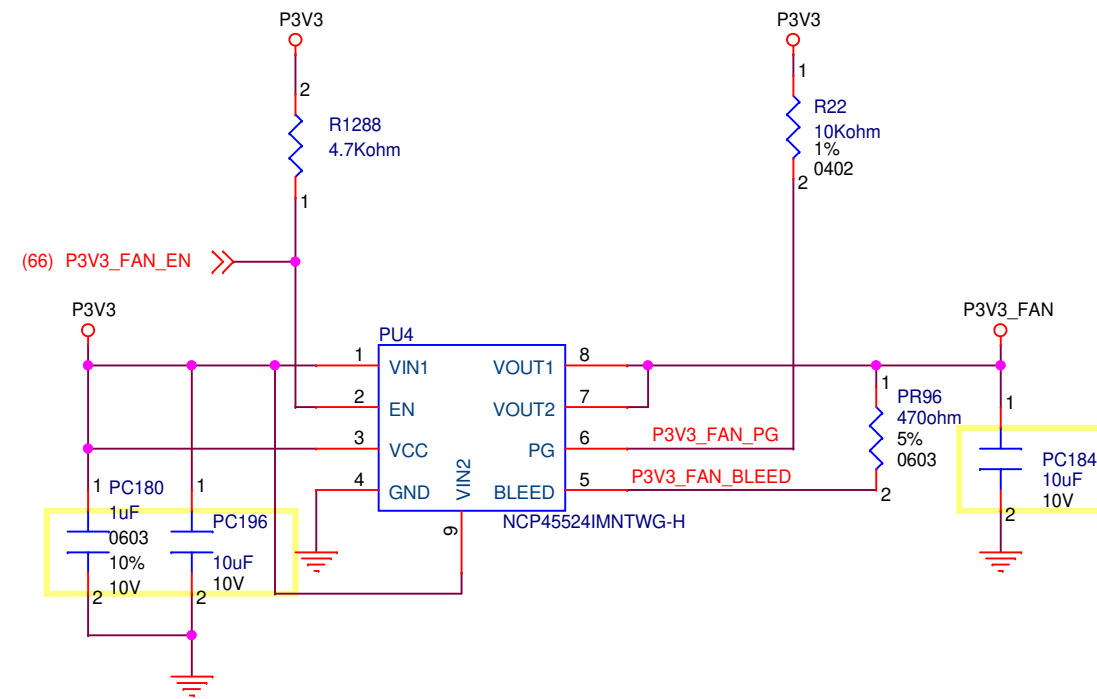
UfiSpace Co., Ltd.	
Title 093_12V to ROV/355A_9-12	
Document Number: PCB P/N: T99O142T00	Sheet 93 of 101
	Rev 005



P3V3_I2C_1.6A

Max = 6A

CAD NOTE:
Add divider circuit can make Enable pin not floating,
and to avoid turn on /turn off error action.



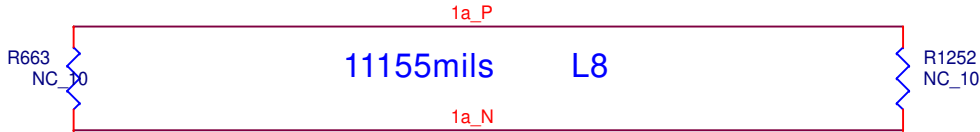
P3V3_FAN_0.6A

Max = 6A

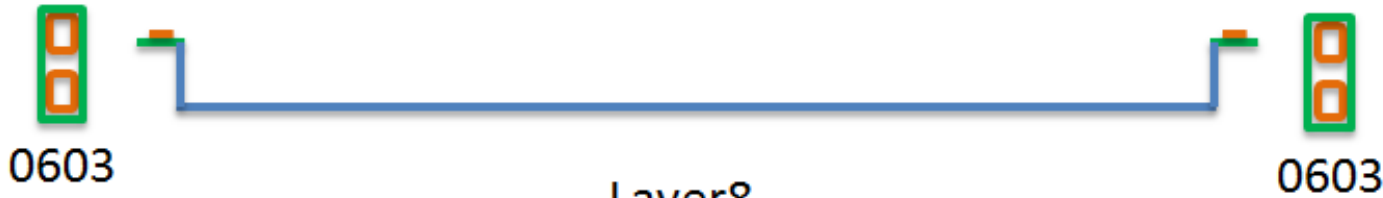
<Core Design>

		UfiSpace Co., Ltd.	
Title 094_3V3 to 3V3_I2C/FAN			
Document Number: PCB P/N: T99O142T00		Sheet 94 of 101	Rev 005

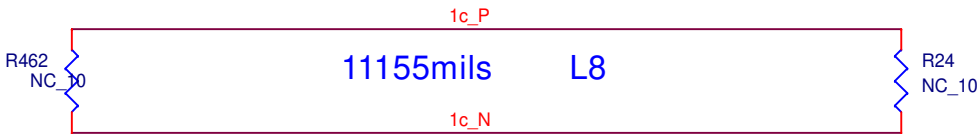
The longest trace ()



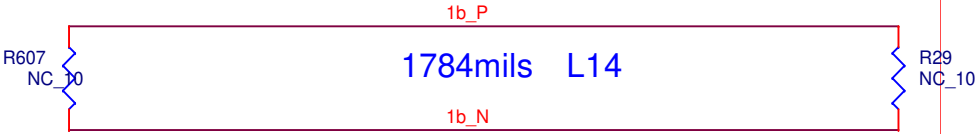
Cross View



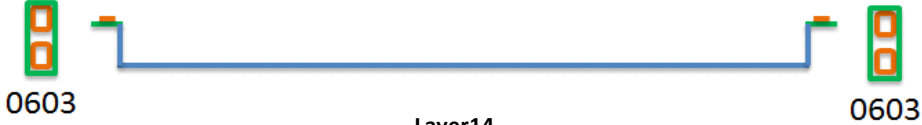
The longest trace with GND Via ()



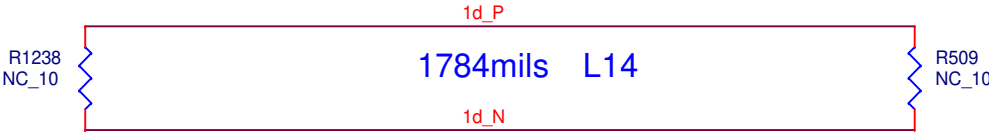
The shortest trace ()



Cross View



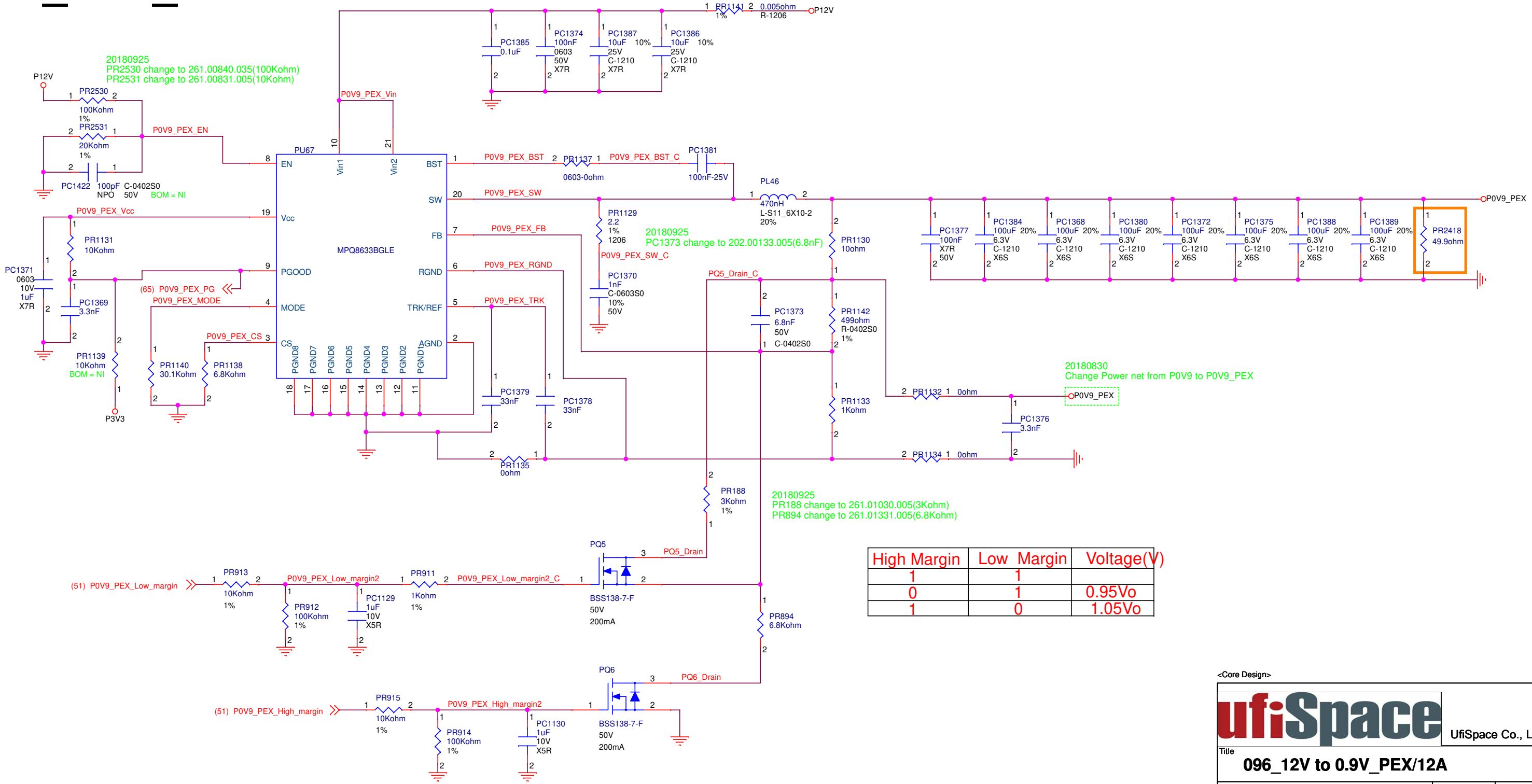
The shortest trace with GND via()



<Core Design>

		UfiSpace Co., Ltd.	
Title 095_Coupon Impendence Test			
Document Number: PCB P/N: T99O142T00		Sheet 95 of 101	Rev 005

P0V9_PEX_12A



<Core Design>

ufiSpace

UfiSpace Co., Ltd.

Title

096_12V to 0.9V_PEX/12A

Document Number:

T990142T00

PCB P/N:

T990142T00

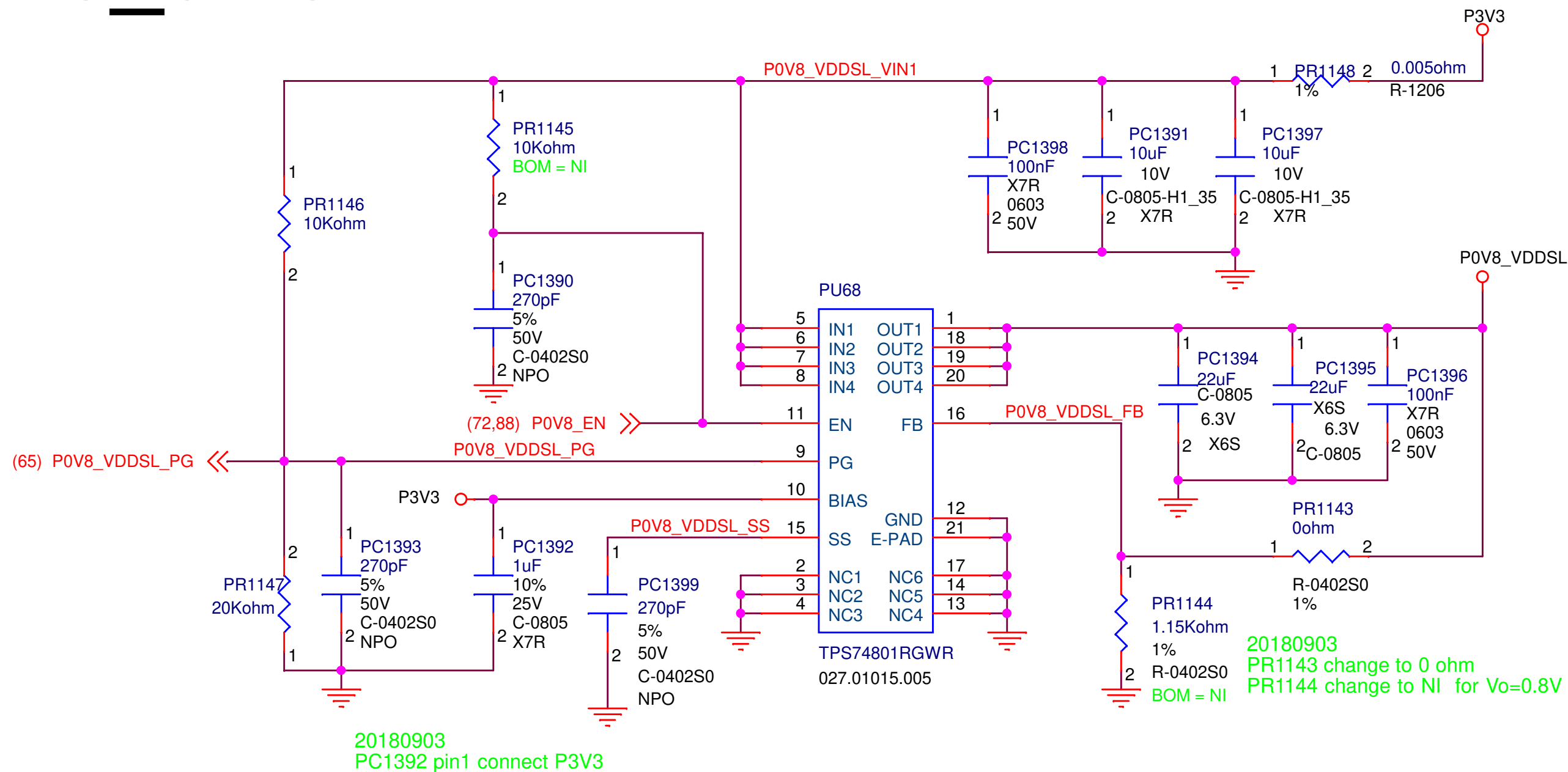
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P0V8_0.75A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>



UfiSpace Co., Ltd.

Title

097_3V3 to 0V8_VDDSL/0.75A

Document Number:

PCB P/N:

T99O142T00

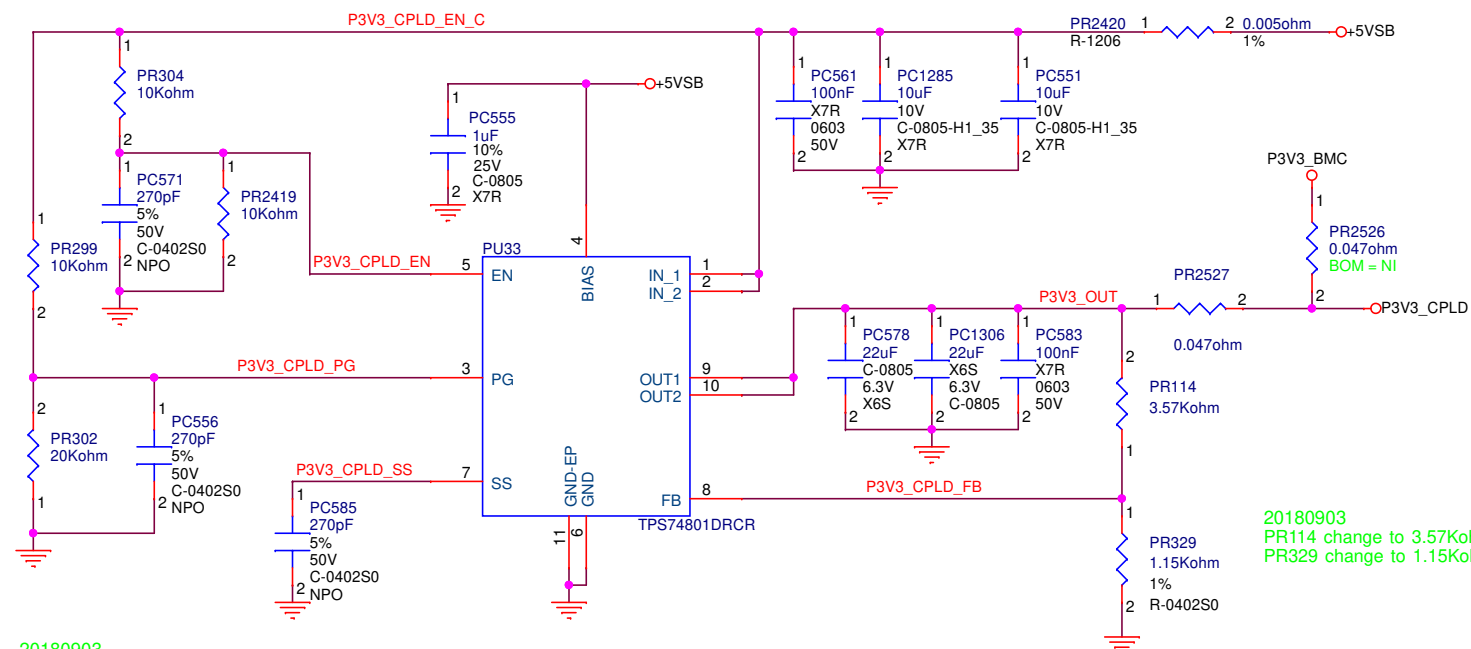
Sheet

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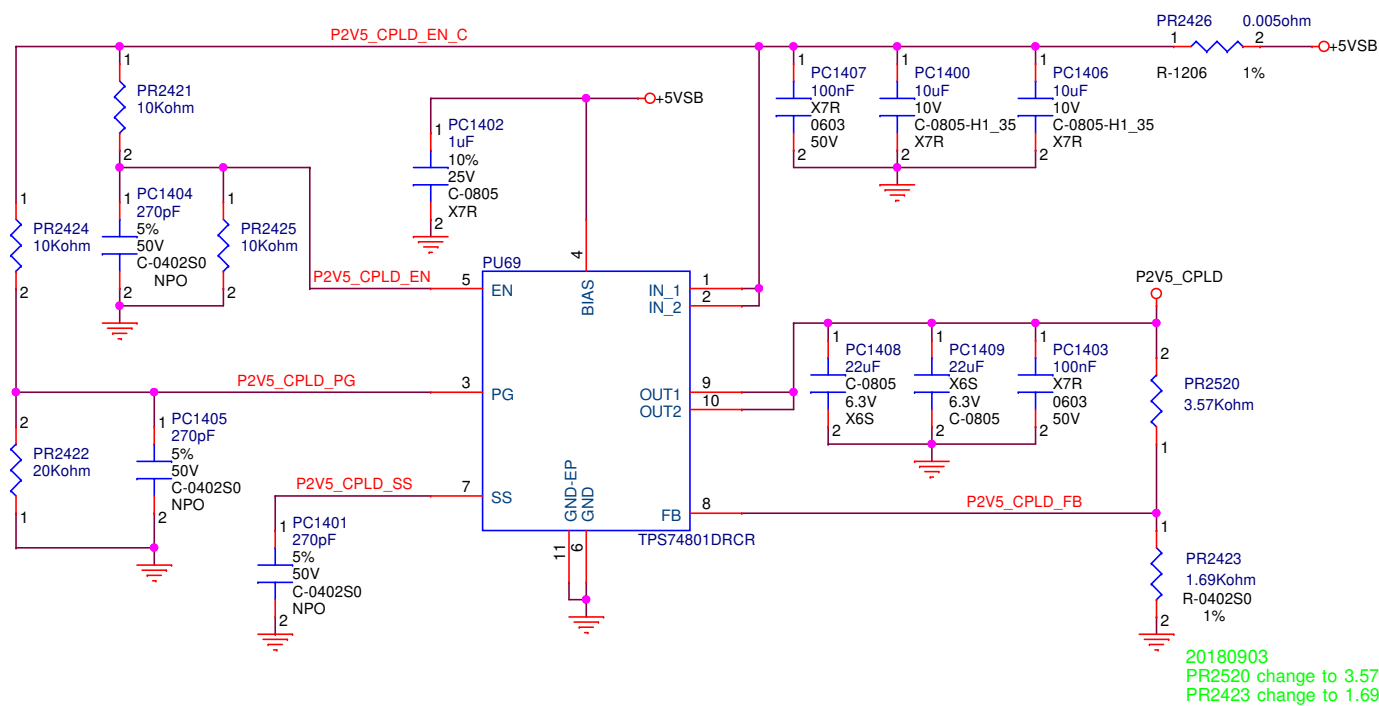
Rev

005

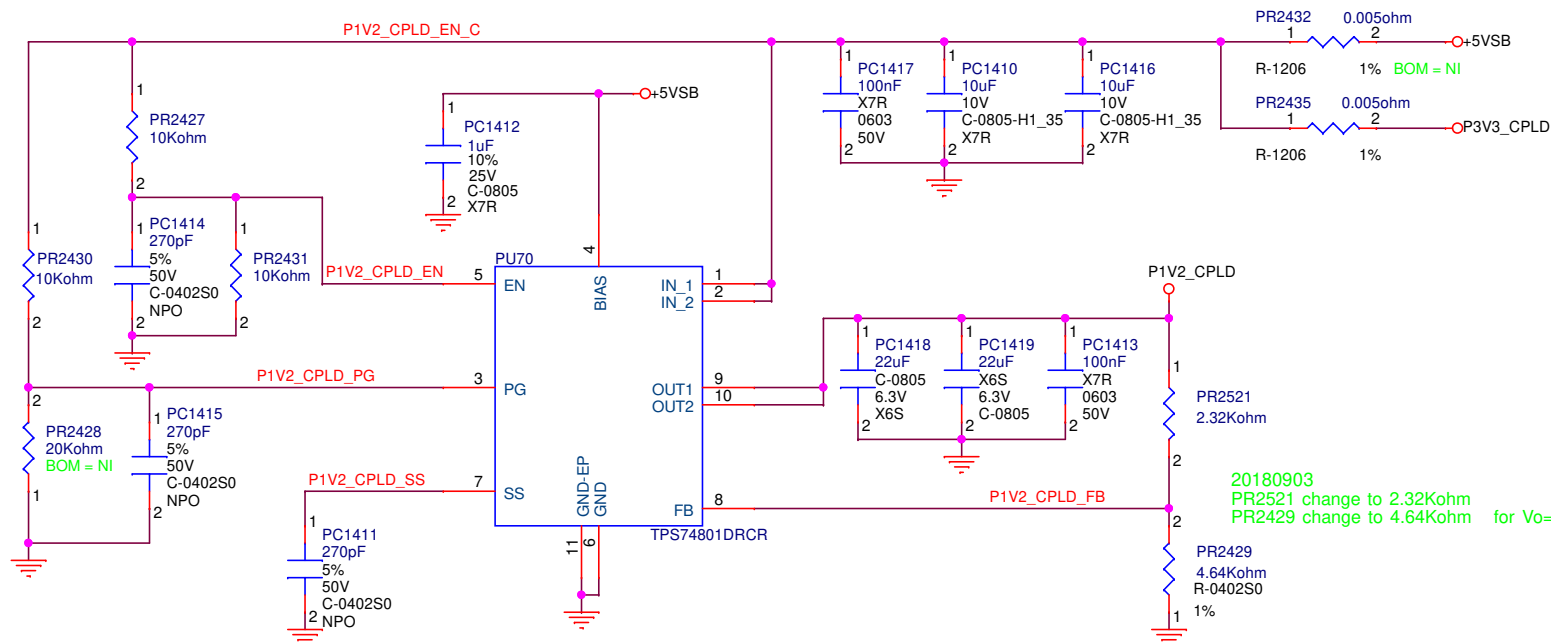
CPLD_POWER



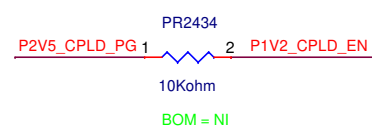
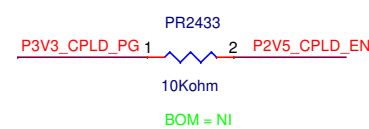
20180903
Insert PR302,PR2422



20180903
PR2520 change to 3.57Kohm
PR2423 change to 1.69Kohm for Vo=2.5V



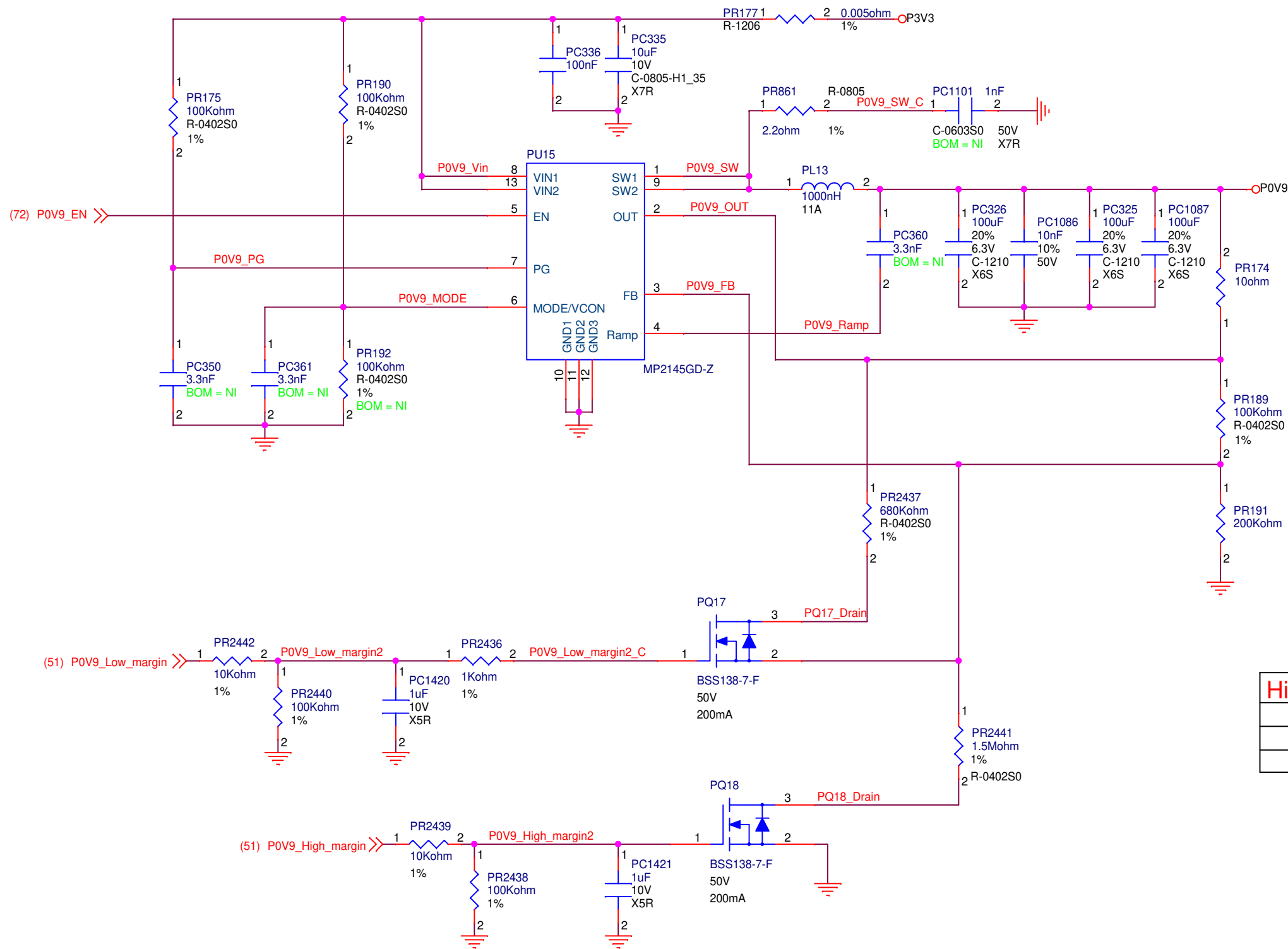
20180903
PR2521 change to 2.32Kohm
PR2429 change to 4.64Kohm for Vo=1.2V



<Variant Name>



P0V9_1A



High Margin	Low Margin	Voltage(V)
1	1	
0	1	0.95Vo
1	0	1.05Vo

<Core Design>



UfiSpace Co., Ltd.

Title

099_3V3 to 0.9V/1A

Document Number:

T99O142T00

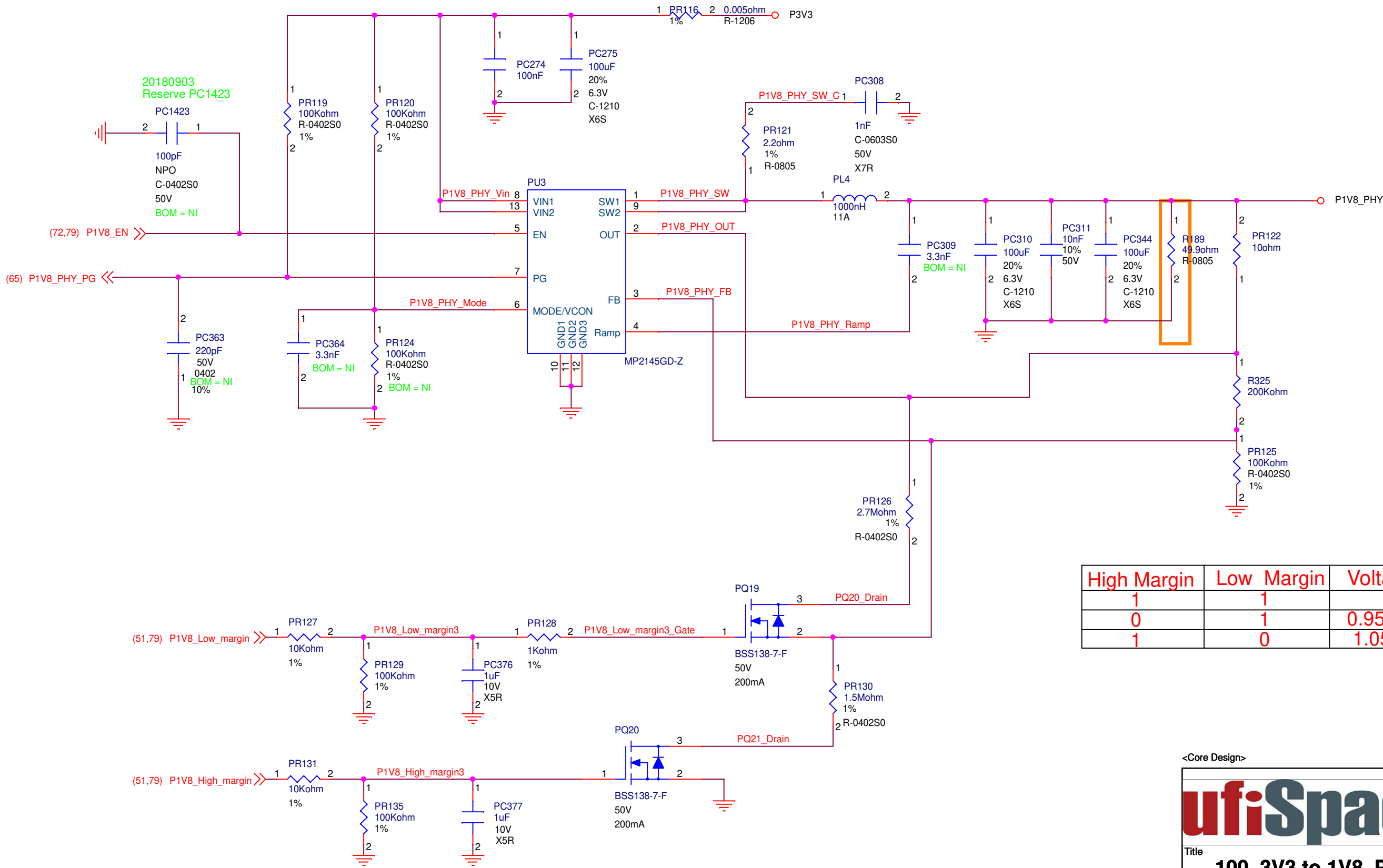
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P1V8_PHY_0.5A



<Core Design>

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UfiSpace Co., Ltd.

Title

100_3V3 to 1V8_PHY/0.5A

Document Number:
PCB P/N:

T99O142T00

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